NLAS7222B, NLAS7222C

High-Speed USB 2.0 (480 Mbps) DPDT Switches

ON Semiconductor's NLAS7222B and NLAS7222C are part of a series of analog switch circuits that are produced using the company's advanced sub−micron CMOS technology, achieving industry−leading performance.

Both the NLAS7222B and NLAS7222C are 2− to 1−port analog switches. Their wide bandwidth and low bit−to−bit skew allow them to pass high−speed differential signals with good signal integrity. Each switch is bidirectional and offers little or no attenuation of the high−speed signals at the outputs. Industry−leading advantages include a propagation delay of less than 250 ps, resulting from its low channel resistance and low I/O capacitance. Their high channel−to−channel crosstalk rejection results in minimal noise interference. Their bandwidth is wide enough to pass High−Speed USB 2.0 differential signals (480 Mb/s).

Features

- R_{ON} is Typically 8.0 Ω at V_{CC} = 3.3 V
- Low Crosstalk: −30 dB @ 250 MHz
- Low Current Consumption: 1.0 μA
- Channel On−Capacitance: 8.0 pF (Typical)
- V_{CC} Operating Range: 1.65 V to 4.5 V
- > 700 MHz Bandwidth (or Data Frequency)
- These are Pb−Free Devices

Typical Applications

- Differential Signal Data Routing
- USB 2.0 Signal Routing

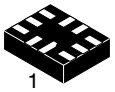
Important Information

- Continuous Current Rating Through Each Switch ±300 mA
- 8 kV I/O to GND ESD Protection

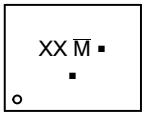
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



UQFN10
CASE 488AT



XX = Device Code
7222B = AS
7222C = AT
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

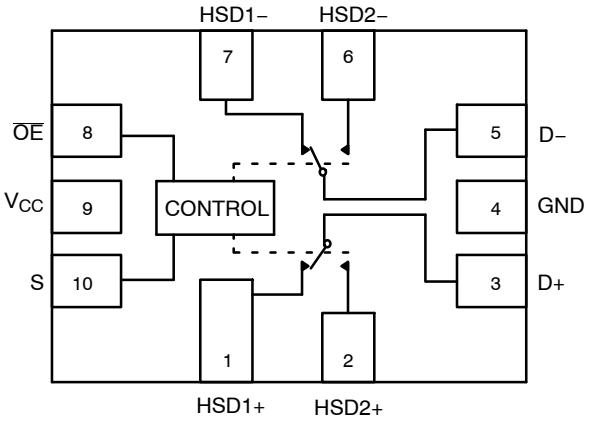


Figure 1. Pin Connections and Logic Diagram
(NLAS7222B, Top View)

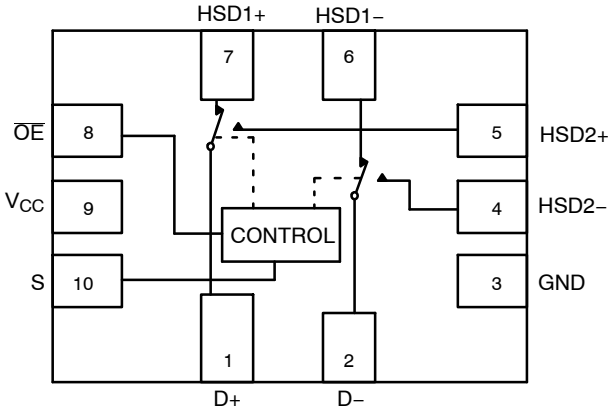


Figure 2. Pin Connections and Logic Diagram
(NLAS7222C, Top View)

Table 1. PIN DESCRIPTION

Pin	Function
S	Select Input
$\overline{OE}$	Output Enable
HSD1+, HSD1−, HSD2+, HSD2−, D+, D−	Data Ports

Table 2. TRUTH TABLE

$\overline{OE}$	S	HSD1+, HSD1−	HSD2+, HSD2−
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	−0.5 to +5.5	V
V_{IS}	HSD1+, HSD1− HSD2+, HSD2−	Analog Signal Voltage	−0.5 to V_{CC} + 0.3	V
	D+, D−		−0.5 to +5.5	
V_{IN}	S, $\overline{OE}$	Control Input Voltage, Output Enable Voltage	−0.5 to +5.5	V
I_{CC}	V_{CC}	Positive DC Supply Current	50	mA
T_S		Storage Temperature	−65 to +150	°C
I_{IS_CON}	HSD1+, HSD1− HSD2+, HSD2−, D+, D−	Analog Signal Continuous Current−Closed Switch	±300	mA
I_{IS_PK}	HSD1+, HSD1− HSD2+, HSD2−, D+, D−	Analog Signal Continuous Current 10% Duty Cycle	±500	mA
I_{IN}	S, $\overline{OE}$	Control Input Current, Output Enable Current	±20	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
V_{CC}		Positive DC Supply Voltage	1.65	4.5	V
V_{IS}	HSD1+, HSD1− HSD2+, HSD2−	Analog Signal Voltage	GND	V_{CC}	V
	D+, D−		GND	4.5	
V_{IN}	S, $\overline{OE}$	Control Input Voltage, Output Enable Voltage	GND	V_{CC}	V
T_A		Operating Temperature Range	−40	+85	°C

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

ESD PROTECTION

Symbol	Parameter	Value	Unit
ESD	Human Body Model – All Pins	2.0	kV
ESD	Human Body Model – I/O to GND	8.0	kV

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT, OUTPUT ENABLE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
V_{IH}	S, $\overline{OE}$	Control Input, Output Enable HIGH Voltage (See Figure 3)		2.7 3.3 4.2	1.3 1.4 1.6	–	–	V
V_{IL}	S, $\overline{OE}$	Control Input, Output Enable LOW Voltage (See Figure 3)		2.7 3.3 4.2	–		0.4 0.4 0.5	V
I_{IN}	S, $\overline{OE}$	Control Input, Output Enable Leakage Current	$0 \le V_{IS} \le V_{CC}$	1.65 – 4.5	–	–	±1.0	μA

SUPPLY AND LEAKAGE CURRENT (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
I_{CC}	V_{CC}	Quiescent Supply Current	$V_{IS} = V_{CC}$ or GND; I_{OUT} = 0 A	1.65 – 4.5	–	–	1.0	μA
I_{CCT}	V_{CC}	Increase in I_{CC} per Control Voltage	V_{IN} = 2.6 V	3.6	–	–	10	μA
I_{OZ}	HSD1+, HSD1– HSD2+, HSD2–	OFF State Leakage Current	$0 \le V_{IS} \le V_{CC}$	1.65 – 4.5	–	–	±1.0	μA
I_{OFF}	D+, D–	Power OFF Leakage Current	$0 \le V_{IS} \le 4.5$ V	0	–	–	±1.0	μA

HIGH SPEED ON RESISTANCE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
R_{ON}		On–Resistance	V_{IS} = 0 V to 0.4 V, I_{ON} = 8 mA	2.7 3.3 4.2	–	9.0 8.0 7.0	12 10 8.0	Ω
R_{FLAT}		On–Resistance Flatness	V_{IS} = 0 V to 1.0 V, I_{ON} = 8 mA	2.7 3.3 4.2	–	1.6 1.5 1.4	–	Ω
ΔR_{ON}		On–Resistance Matching	V_{IS} = 0 V to 0.4 V, I_{ON} = 8 mA	2.7 3.3 4.2	–	1.05 0.85 0.65	–	Ω

DC ELECTRICAL CHARACTERISTICS (continued)

FULL SPEED ON RESISTANCE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
R_{ON}		On−Resistance	V_{IS} = 0 V to V_{CC}, I_{ON} = 8 mA	2.7 3.3 4.2		9.0 8.5 7.5	12 10.5 8.5	Ω
R_{FLAT}		On−Resistance Flatness	V_{IS} = 0 V to 1.0 V, I_{ON} = 8 mA	2.7 3.3 4.2		1.6 1.5 1.4		Ω
ΔR_{ON}		On−Resistance Matching	V_{IS} = 0 V to V_{CC}, I_{ON} = 8 mA	2.7 3.3 4.2		2.20 2.45 2.65		Ω

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
t_{ON}	Closed to Open	Turn−ON Time		1.65 – 4.5	–	14	30	ns
t_{OFF}	Open to Closed	Turn−OFF Time		1.65 – 4.5	–	10	20	ns
t_{BBM}		Break−Before−Make Delay		1.65 – 4.5	3.0	4.4	7.0	ns
BW		−3 dB Bandwidth	C_L = 5 pF	1.65 – 4.5	–	500	–	MHz
			C_L = 0 pF		–	750	–	

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
O_{IRR}	Open	OFF−Isolation	f = 250 MHz	1.65 – 4.5	–	−22	–	dB
X_{TALK}	HSD1+ to HSD1−	Non−Adjacent Channel Crosstalk	f = 250 MHz	1.65 – 4.5	–	−30	–	dB

NLAS7222B CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	–40°C to +85°C			Unit
				Min	Typ	Max	
C_{IN}	S, $\overline{OE}$	Control Pin Input Capacitance	V_{CC} = 0 V	–	3.0	–	pF
C_{ON}	D+ to HSD1+ or HSD2+	ON Capacitance	V_{CC} = 3.3 V; $\overline{OE}$ = 0 V S = 0 V or 3.3 V	–	8.0	–	pF
C_{OFF}	HSD1n or HSD2n	OFF Capacitance	V_{CC} = V_{IS} = 3.3 V; $\overline{OE}$ = 0 V S = 3.3 V or 0 V	–	4.5	–	pF

NLAS7222C CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	–40°C to +85°C			Unit
				Min	Typ	Max	
C_{IN}	S, $\overline{OE}$	Control Pin, Output Enable Input Capacitance	V_{CC} = 0 V	–	3.0	–	pF
C_{ON}	D+ to HSD1+ or HSD2+	ON Capacitance	V_{CC} = 3.3 V; $\overline{OE}$ = 0 V S = 0 V or 3.3 V	–	10	–	pF
C_{OFF}	HSD1n or HSD2n	OFF Capacitance	V_{CC} = V_{IS} = 3.3 V; $\overline{OE}$ = 3.3 V S = 3.3 V or 0 V	–	5.5	–	pF

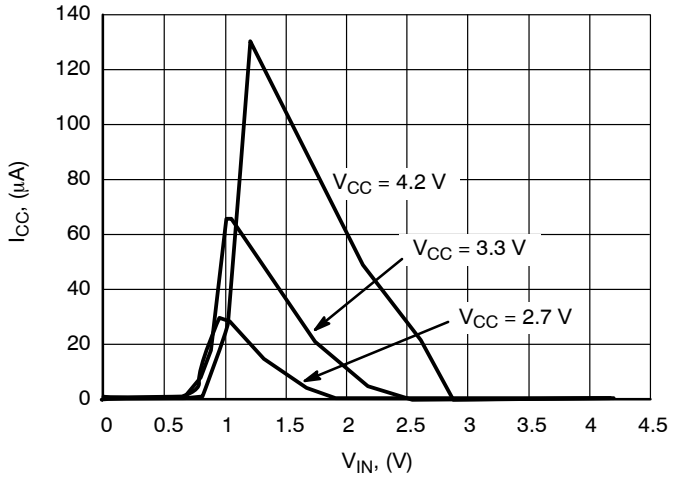


Figure 3. I_{CC} vs. V_{IN}

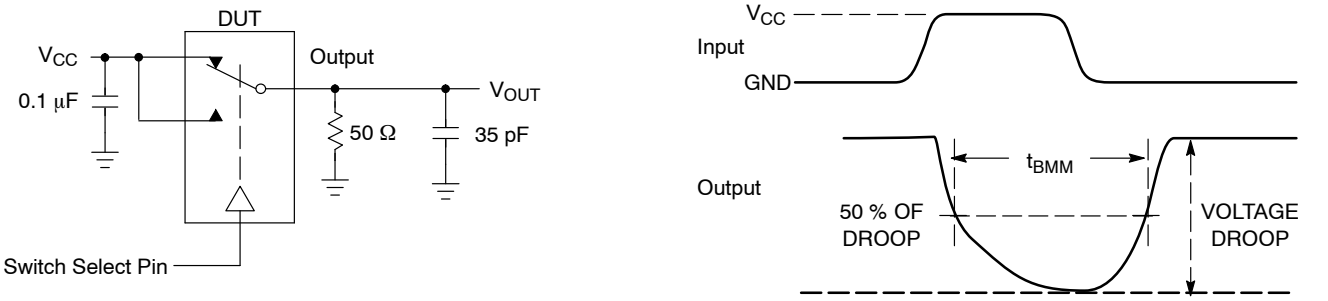


Figure 4. t_{BBM} (Time Break−Before−Make)

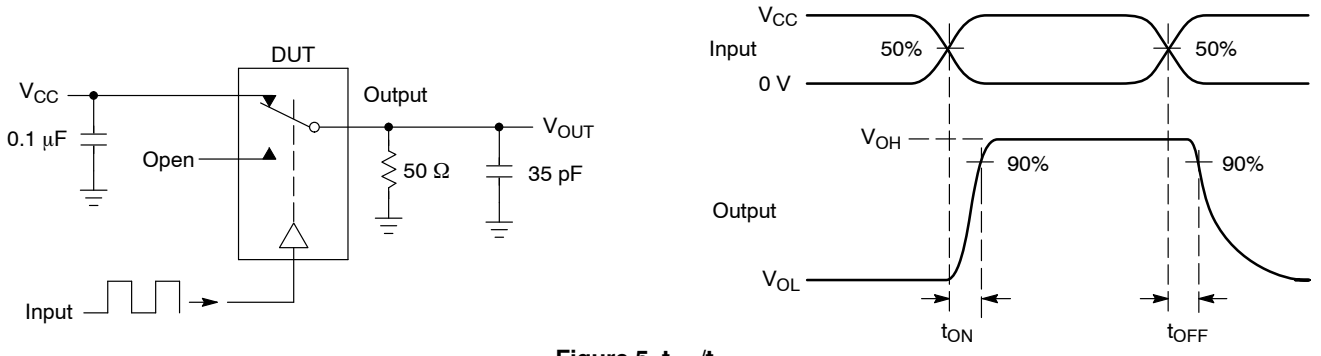


Figure 5. t_{ON}/t_{OFF}

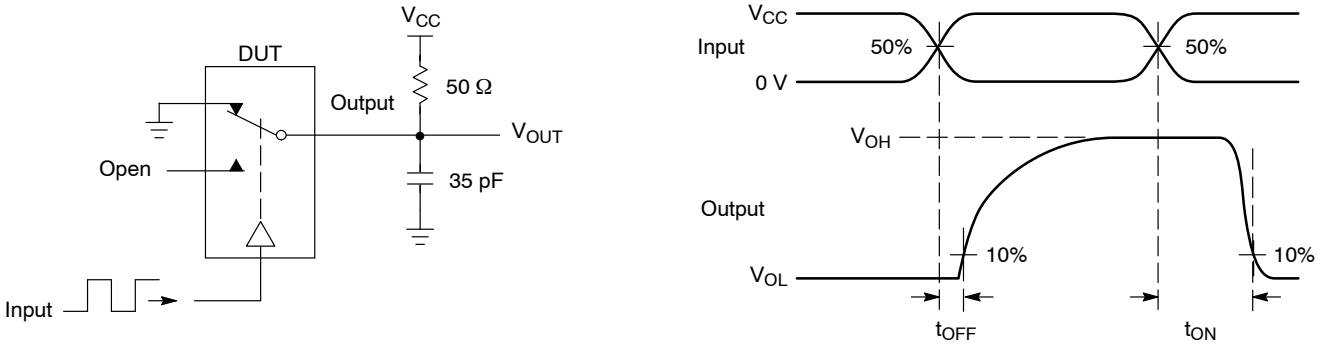
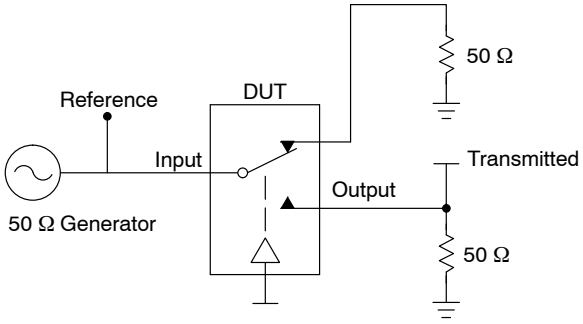


Figure 6. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

APPLICATIONS INFORMATION

The low on resistance and capacitance of the NLAS7222B provides for a high bandwidth analog switch suitable for applications such as USB data switching. Results for the USB 2.0 signal quality tests will be shown in this section, along with a description of the evaluation test board. The data for the eye diagram signal quality and jitter tests verifies that the NLAS7222B can be used as a data switch in low, full and high speed USB 2.0 systems.

Figures 8, 9 and 10 provide a description of the test evaluation board. The USB tests were conducted per the procedures provided by the USB Implementers Forum (www.usb.org), the industry group responsible for defining the USB certification requirements. The test patterns were generated by a PC and MATLAB software, and were inputted to the analog switch through USB connectors J1 (HSD1) or J2 (HSD2). A USB certified device was plugged into connector J4 to function as a data transceiver. The high speed and full speed tests used a flash memory device, while the low speed tests used a mouse. Test connectors J3 and J5 provide a direct connection of the USB device and were used to verify that the analog switch does not distort the data signals.

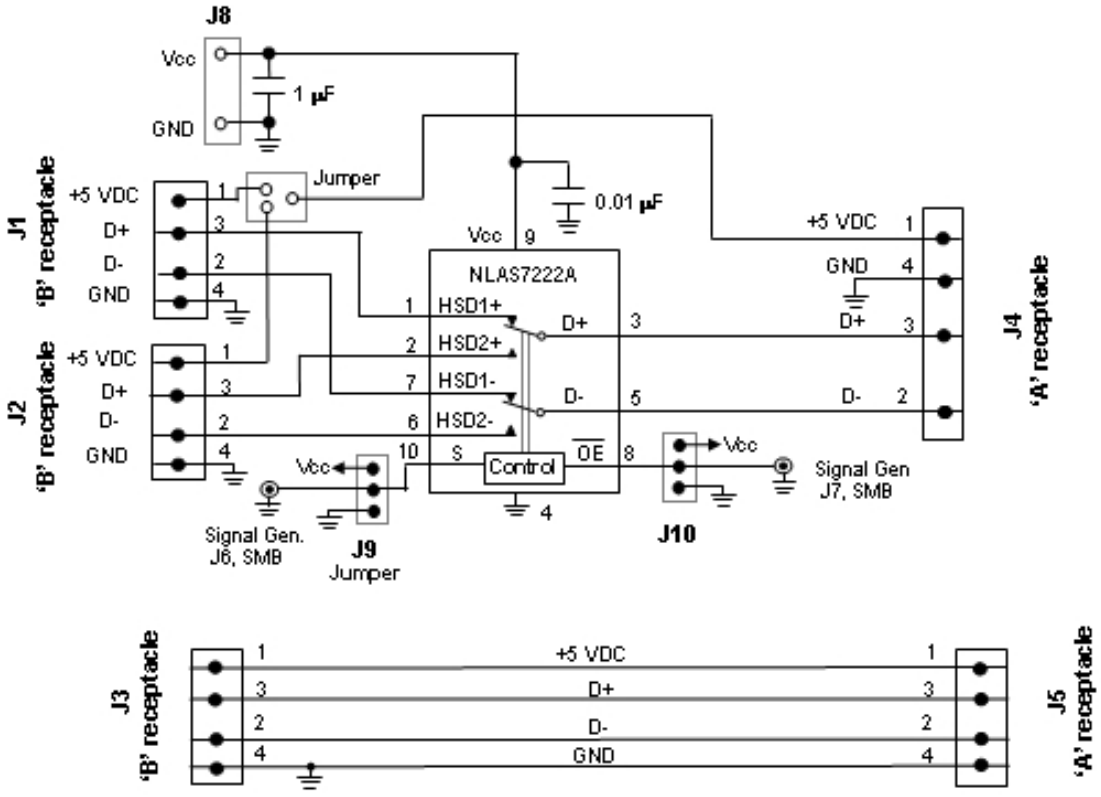


Figure 8. Schematic of the NLAS7222B USB Demo Board

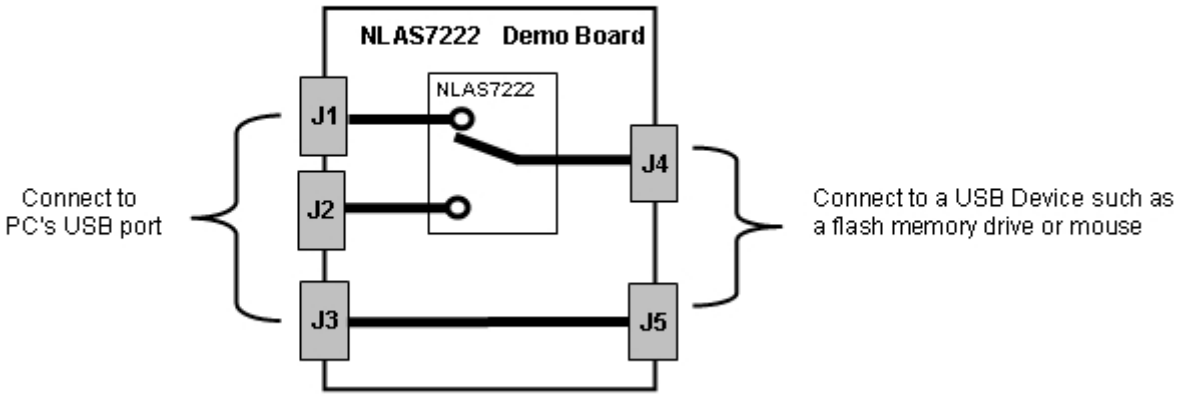


Figure 9. Block Diagram of the NLAS7222B USB Demo Board

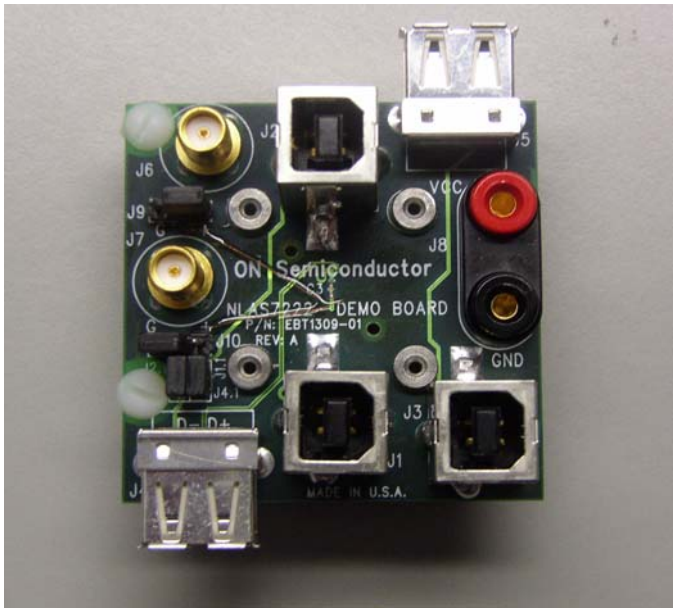


Figure 10. Photograph of the NLAS7222B USB Demo Board

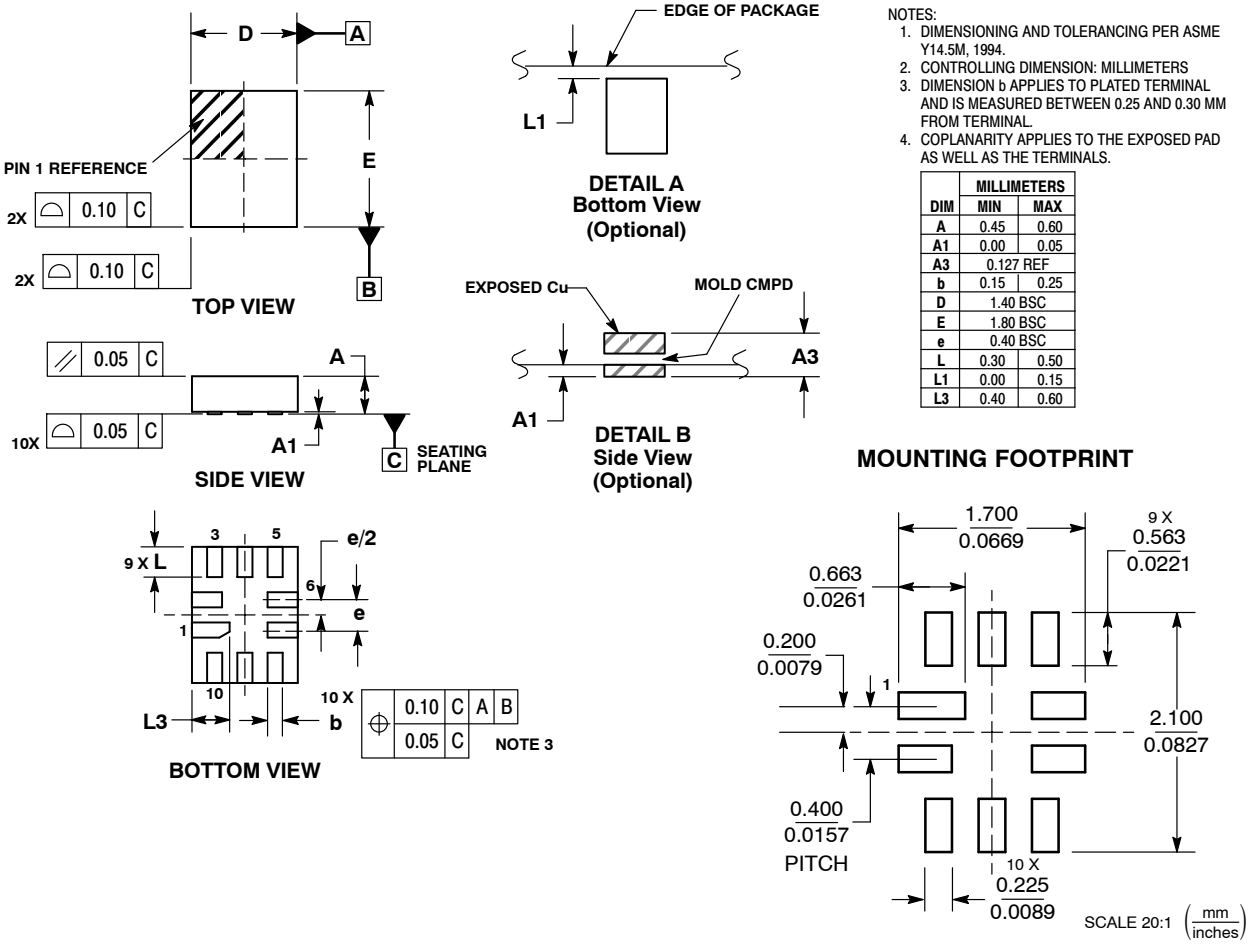
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NLAS7222BMUTAG	AS	UQFN10 (Pb−Free)	3000 / Tape & Reel
NLAS7222BMUTBG	AS	UQFN10 (Pb−Free)	3000 / Tape & Reel
NLAS7222CMUTBG	AT	UQFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

UQFN10, 1.4x1.8, 0.4P
CASE 488AT−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

MOUNTING FOOTPRINT

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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