

PIC18F26K20/46K20 Rev. A4, A5 Silicon Errata and Data Sheet Clarification

The PIC18F26K20/46K20 family devices that you have received conform functionally to the current Device Data Sheet (DS41303H), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC18F26K20/46K20 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on [page 9](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
 - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F26K20/46K20 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾ (11-bit)	Revision ID for Silicon Revision ⁽²⁾ (5-bit)	
		A4	A5
PIC18F26K20	100h	0x06	0x07
PIC18F46K20	101h	0x06	0x07

- Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:DEVREV".
- 2:** Refer to the "*PIC18F2XK20/4XK20 Flash Programming Specification*" (DS41297) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A4	A5
ECCP	ECCP Modes	1.	Changing ECCP mode may cause a false capture of TMR1 value.	X	X
ECCP	Full-Bridge	2.	Compromised dead band.	X	X
MSSP I ² C	I ² C	3.	Slower slew rate than I ² C specifications.	X	X
ADC	ADC Conversion	4.	Offset error is 3 LSb typical and 7 LSb maximum.	X	X
MSSP I ² C	I ² C	5.	False ACK generated when SSPOV bit is set and a matching address is clocked-in.	X	X
MSSP I ² C	I ² C Master	6.	The first high-clock cycle following a clock stretching event may be shorter than half the clock period.	X	X
MSSP I ² C	I ² C Master Baud Rate	7.	Unexpected operation may occur if SSPADD is set to a value lower than 0x03.	X	X
MSSP SPI	SPI Clock	8.	First SPI clock may be short if SPI clock is configured to Timer2output/2.	X	X
MSSP SPI	SPI Master	9.	When CKE is cleared and SMP is set, the last bit of incoming data will not be sampled properly.	X	X
MSSP SPI	SPI Master	10.	SSPBUF will reload the SSPSR output on every SS pin toggle, if CKE is set.	X	X
MSSP SPI	SPI Master	11.	Erroneous output on SCK pin for CKE = 1 and CKP = 0.	X	X
EUSART	Synchronous mode	12.	Duty cycle of CK is skewed by one baud count if SPBRG is set to an odd number.	X	X
EUSART	Transmit Buffer	13.	Data corruption may occur if TXREG is written while TX shift register has some characters in it for SPBRG = 3.	X	X
EUSART	Transmit mode	14.	Improper clock behavior for SPBRG = 0.	X	X
System Clocks	HFINTOSC	15.	HFINTOSC output frequency is 16 MHz ± 3%, 25°C to 85°C.	X	X
POR/BOR	Power-on Reset	16.	Unexpected code execution may occur below the BOR range.	X	X
POR	Power-on Reset	17.	POR may release below the rearm voltage for certain BOR voltages.	X	X
POR	Power-on Reset	18.	Part may stay in Reset state if POR triggers and then VDD rises faster than 7500 volts per second.	X	X
Clocks	EC mode	19.	EC Mode operation is limited to a maximum of 48 MHz.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A4	A5
Comparators	Input Offset Voltage	20.	Comparator input offset voltage range increases as the Common mode voltage decreases and may degrade over the lifetime of the part, accelerated by high temperature.	X	X
Comparators	Comparator Output	21.	The CxOUT is forced to zero when the CxON bit is clear, irrespective of the CxPOL bit setting.	X	X
Data EEPROM Memory	Endurance	22.	The write/erase endurance of Data EE Memory is limited to 10K cycles.	X	X
Program Flash Memory	Endurance	23.	The write/erase endurance of the PFM is limited to 1K cycles when VDD is above 3V.	X	X
Input/Output (PIC18F26K20 only)	I/O Pins	24.	Reading PORTE bit 3 always returns 0.	X	X
Timer1	Timer Interrupt	25.	False interrupt may occur in Asynchronous mode.	X	X
Timer1/3	Timer Interrupt	26.	In Asynchronous mode a false interrupt may occur if the clock arrives too soon following a firmware write to the TMR registers. Also, a switch from Synchronous to Asynchronous mode can cause it.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A5).

1. Module: ECCP

Changing the CCP1M<3:0> bits of CCP1CON may cause the CCPR1H and CCPR1L registers to capture the value of Timer1.

Work around

Halt Timer1 before changing ECCP mode. Reload Timer1 with desired value after ECCP is setup and before Timer1 is restarted.

Affected Silicon Revisions

A4	A5				
X	X				

2. Module: ECCP

Changing direction in Full-Bridge mode does not insert dead time between changing the active drivers in common legs of the bridge.

Work around

None.

Affected Silicon Revisions

A4	A5				
X	X				

3. Module: MSSP I²C

Slew rate is slower than I²C specifications when the SLRCON<2> bit is set.

Work around

Clear SLRCON<2> bit when using the I²C peripheral.

Affected Silicon Revisions

A4	A5				
X	X				

4. Module: ADC

Offset error is 3 LSb typical, 7 LSb maximum, including an acquisition time dependent component (~2 LSb).

Work around

The time dependent error is insignificant when the time between conversions is less than 100 ms. When the time since the previous conversion is greater than 100 ms then take two ADC conversions and discard the first.

Affected Silicon Revisions

A4	A5				
X	X				

5. Module: MSSP I²C

If a new address byte is received while the BF flag is set, the SSPOV bit is set and an ACK is not generated, both of which are proper operation. If only the SSPOV bit is set (BF flag was cleared) and a matching address is clocked in, that received byte will be loaded into the SSPBUF register and an ACK will be generated, both of which are improper operation.

Work around

None.

Affected Silicon Revisions

A4	A5				
X	X				

6. Module: MSSP I²C

In Master I²C mode, when a slave device releases the clock after holding it low (clock stretching), the pulse width of the first high clock cycle may be shorter than half the clock period.

Work around

None.

Affected Silicon Revisions

A4	A5				
X	X				

7. Module: MSSP I²C

In Master I²C mode, baud rates obtained by setting SSPADD to a value less than 0x03 will cause unexpected operation.

Work around

Ensure SSPADD is set to a value greater than or equal to 0x04.

Affected Silicon Revisions

A4	A5				
X	X				

8. Module: MSSP SPI

When the SPI clock is configured for Timer2 output/2 (SSPCON1<3:0> = 0011), the first SPI high time may be short.

Work around

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

Affected Silicon Revisions

A4	A5				
X	X				

9. Module: MSSP SPI

In SPI Master mode, when the CKE bit is cleared and the SMP bit is set, the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

A4	A5				
X	X				

10. Module: MSSP SPI

In SPI Master mode, when CKE bit is set, the SSPBUF will reload the SSPSR output shift register on every high-to-low transition of the \overline{SS} pin.

Work around

Avoid using the \overline{SS} pin when the CKE bit is set and the MSSP is configured for SPI Master mode.

Affected Silicon Revisions

A4	A5				
X	X				

11. Module: MSSP SPI

When SPI is enabled in Master mode with CKE = 1 and CKP = 0, a 1/FOSC wide pulse will occur on the SCK pin.

Work around

Configure the SCK pin as an input until after the MSSP is setup.

Affected Silicon Revisions

A4	A5				
X	X				

12. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to an odd number, the duty cycle of the CK output will be skewed by one baud clock count.

Work around

High values of SPBRG will minimize the effect of this anomaly.

Affected Silicon Revisions

A4	A5				
X	X				

13. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to 3 and the TXREG is written while the previous character is still in the TX shift register, the LS bit of the TXREG character may be corrupted during transmission.

Work around

When SPBRG is set to 3, wait until the TRMT bit of the TXSTA register is set before loading TXREG with the next character to be transmitted.

Affected Silicon Revisions

A4	A5				
X	X				

14. Module: EUSART

In Synchronous Master mode, if the SPBRG register is equal to 0, when the TXEN bit is set, then writing to TXREG will properly start transmission. However, the clock will be improperly out of phase with the data bits and the clock will not stop at the end of the character transmission.

Work around

Set SPBRG register to non-zero value before setting the TXEN bit.

Affected Silicon Revisions

A4	A5				
X	X				

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15. Module: System Clocks

HFINTOSC output frequency is 16 MHz \pm 3%, 25°C to 85°C.

Work around

None.

Affected Silicon Revisions

A4	A5				
X	X				

16. Module: POR/BOR

The POR rearm voltage may be below the low end of the BOR range causing unexpected code execution below the BOR range.

Work around

Use external power monitor to hold device in Reset below 1.1 Volts.

Affected Silicon Revisions

A4	A5				
X	X				

17. Module: POR

The POR may release around 0.8 volts (below the POR rearm voltage of 1.2V nominal) when VDD rises from below either 0.60V when BOR is not enabled, or 0.33V when BOR is enabled.

Work around

Use Power-up Timer when operating with the EC, EXTRC or HFINTOSC oscillator modes. Ensure that VDD rise time is less than the Power-up Timer time.

Affected Silicon Revisions

A4	A5				
X	X				

18. Module: POR

The part may hang in the Reset state when VDD falls to the POR rearm threshold of approximately 1.2 volts then rises at a rate faster than 7500 volts per second to the operating range. Recovery from the hung state is possible only by first lowering VDD to below the POR rearm threshold followed by raising VDD to the operating range.

Work around

Slow VDD rise time by adding series resistance between the voltage supply and the VDD pin. VDD bypassing should remain on the pin side of the series resistor.

Affected Silicon Revisions

A4	A5				
X	X				

19. Module: Clocks

EC Mode operation is limited to a maximum of 48 MHz.

Work around

Use HS Clock mode for external clocking above 48 MHz.

Affected Silicon Revisions

A4	A5				
X	X				

20. Module: Comparators

Comparator input offset voltage is \pm 25 mV and may degrade over the lifetime of the part accelerated by high temperature. The offset voltage increases as the common-mode voltage decreases with the following characteristics: Offset is \pm 25 mV when the common-mode voltage is VDD; The offset is up to \pm 50 mV when the common-mode voltage is VDD/2; The offset is greater than \pm 50 mV when the common-mode voltage is 0V.

Work around

None.

Affected Silicon Revisions

A4	A5				
X	X				

21. Module: Comparators

When the CxON bit is clear, the output from the comparator will be properly forced to zero, but the CxPOL bit will improperly have no effect on the CxOUT bit. This prevents presetting the comparator change-on-interrupt mismatch latches as described in the data sheet.

Work around

Configure one of the unused comparator input channels as a digital output. Use that digital output to manipulate the comparator output to the desired CxOUT non-interrupt level. When the comparator

is then set to the desired inputs, the mismatch latches will be preset to the non-interrupt level and the CxIF flag can then be cleared.

Affected Silicon Revisions

A4	A5				
X	X				

22. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

A4	A5				
X	X				

23. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when VDD is above 3V. Endurance degrades when VDD is below 3V.

Work around

For data tables in Program Flash Memory, use the error correction method that stores data in multiple locations.

Affected Silicon Revisions

A4	A5				
X	X				

24. Module: Input/Output (PIC18F26K20 only)

Reading PORTE bit 3 always returns 0.

Work around

None.

Affected Silicon Revisions

A4	A5				
X	X				

25. Module: Timer1

In Asynchronous Counter mode, a false interrupt may occur on the first rising T1CKI clock edge after writing the TMR1H or TMR1L register.

Work around

Examine the TMR1H:TMR1L register pair in the Interrupt Service Routine (ISR). If the TMR1H:TMR1L register pair is less than the preset value then service the interrupt. Otherwise, disregard the interrupt and only clear the Timer1 interrupt flag.

Affected Silicon Revisions

A4	A5				
X	X				

26. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in [Example 1](#).

Affected Silicon Revisions

A4	A5				
X	X				

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EXAMPLE 1: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;           //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                   //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;           //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
//value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                          //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```


Data Sheet Clarifications

The following typographical corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303H):

Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Product Identification System

The temperature range values have been corrected.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X⁽¹⁾</u>	<u>X</u>	<u>XX</u>	<u>XXX</u>	
Device	Tape and Reel Option	Temperature Range	Package	Pattern	
Device:	PIC18F26K20; PIC18F46K20; DSTEMP; PIC18F26K20; DSTEMP; PIC16F887; PIC18F45K20; PIC18F46K20.				Examples: a) PIC18F45K20 - E/P 301 = Industrial temp., PDIP package, QTP pattern #301. b) PIC18F26K20 - I/SO = Industrial temp., SOIC package. c) PIC16F887 - E/P = Extended temp., PDIP package. d) PIC18F46K20 - I/PT = Industrial temp., TQFP package, tape and reel. Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel ⁽¹⁾				
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)				
Package:	PT = TQFP (Thin Quad Flatpack) SS = SSOP SO = SOIC SP = SPDIP (Skinny Plastic DIP) P = PDIP ML = QFN MV = UQFN				
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)				

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APPENDIX A: REVISION HISTORY

Rev A Document (12/08)

First revision of this document.

Rev B Document (12/2014)

Added Module 26.

Rev C Document (9/2015)

Updated errata to new format.

Data Sheet Clarifications:

Added Module 1: Product Identification System.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Fax: 44-118-921-5820

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