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June 2016

# FDMD84100

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET

100 V, 21 A, 20 mΩ

### Features

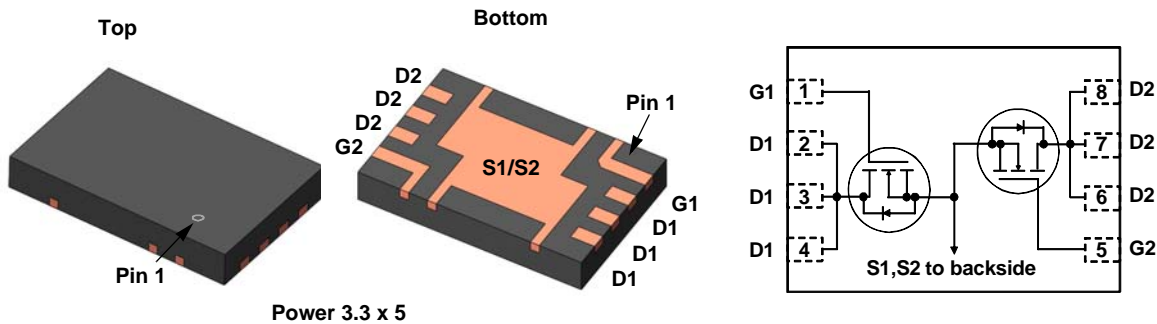
- Max  $r_{DS(on)}$  = 20 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 7\text{ A}$
- Max  $r_{DS(on)}$  = 32 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 5.5\text{ A}$
- Ideal for flexible layout in secondary side synchronous rectification
- Termination is Lead-free and RoHS Compliant
- 100% UIL tested

### General Description

This package integrates two N-Channel devices connected internally in common-source configuration. This enables very low package parasitics and optimized thermal path to the common source pad on the bottom. Provides a very small footprint (3.3 x 5 mm) for higher power density.

### Applications

- Isolated DC-DC Synchronous Rectifiers
- Common Ground Load Switches



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

| Symbol         | Parameter  | Rated                          | Units              |
|----------------|--|--------------------------------|--------------------|
| $V_{DS}$       | Drain to Source Voltage                          | 100                            | V                  |
| $V_{GS}$       | Gate to Source Voltage                           | $\pm 20$                       | V                  |
| $I_D$          | Drain Current -Continuous                        | $T_C = 25\text{ °C}$           | 21                 |
|                | -Continuous                                      | $T_A = 25\text{ °C}$ (Note 1a) | 7                  |
|                | -Pulsed  | (Note 4)                       | 80                 |
| $E_{AS}$       | Single Pulse Avalanche Energy                    | (Note 3)                       | 121                |
| $P_D$          | Power Dissipation                                | $T_C = 25\text{ °C}$           | 23                 |
|                | Power Dissipation                                | $T_A = 25\text{ °C}$ (Note 1a) | 2.1                |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to +150                    | $^{\circ}\text{C}$ |

### Thermal Characteristics

|                 |   |     |                      |
|-----------------|---|-----|----------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case              | 5.3 | $^{\circ}\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 60  |                      |

### Package Marking and Ordering Information

| Device Marking | Device    | Package       | Reel Size | Tape Width | Quantity   |
|----------------|-----------|---------------|-----------|------------|------------|
| 84100          | FDMD84100 | Power 3.3 x 5 | 13 "      | 12 mm      | 3000 units |

FDMD84100 Dual N-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

### Off Characteristics

|                                      |   |   |     |    |           |                      |
|--------------------------------------|---|---|-----|----|-----------|----------------------|
| $BV_{DSS}$                           | Drain to Source Breakdown Voltage         | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$                    | 100 |    |           | V                    |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ |     | 74 |           | mV/ $^\circ\text{C}$ |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$                            |     |    | 1         | $\mu\text{A}$        |
| $I_{GSS}$                            | Gate to Source Leakage Current            | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$                        |     |    | $\pm 100$ | nA                   |

### On Characteristics

|  |  |   |   |     |    |                      |
|--|--|---|---|-----|----|----------------------|
| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$                              | 2 | 3.1 | 4  | V                    |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$       |   | -9  |    | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$                           | Static Drain to Source On Resistance                     | $V_{GS} = 10\text{ V}$ , $I_D = 7\text{ A}$                                     |   | 16  | 20 | m $\Omega$           |
|  |  | $V_{GS} = 6\text{ V}$ , $I_D = 5.5\text{ A}$                                    |   | 24  | 32 |                      |
|  |  | $V_{GS} = 10\text{ V}$ , $I_D = 7\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$ |   | 30  | 38 |                      |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DD} = 5\text{ V}$ , $I_D = 7\text{ A}$                                      |   | 17  |    | S                    |

### Dynamic Characteristics

|           |                              |  |     |     |     |          |
|-----------|------------------------------|--|-----|-----|-----|----------|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$<br>$f = 1\text{ MHz}$ |     | 734 | 980 | pF       |
| $C_{oss}$ | Output Capacitance           |  |     | 168 | 225 | pF       |
| $C_{rss}$ | Reverse Transfer Capacitance |  |     | 6.6 | 15  | pF       |
| $R_g$     | Gate Resistance              |  | 0.1 | 1.3 | 3   | $\Omega$ |

### Switching Characteristics

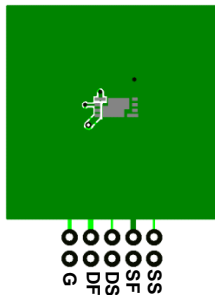
|              |                               |   |  |     |    |    |
|--------------|-------------------------------|---|--|-----|----|----|
| $t_{d(on)}$  | Turn-On Delay Time            | $V_{DD} = 50\text{ V}$ , $I_D = 7\text{ A}$<br>$V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$ |  | 8.4 | 17 | ns |
| $t_r$        | Rise Time                     |   |  | 2.6 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time           |   |  | 14  | 25 | ns |
| $t_f$        | Fall Time                     |   |  | 2.8 | 10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge             |   | $V_{GS} = 0\text{ V to } 10\text{ V}$        |     | 11 | 16 |
|              | Total Gate Charge             | $V_{GS} = 0\text{ V to } 6\text{ V}$  | $V_{DD} = 50\text{ V}$<br>$I_D = 7\text{ A}$ | 7.3 | 11 | nC |
| $Q_{gs}$     | Gate to Source Charge         |   |  | 3.4 |    | nC |
| $Q_{gd}$     | Gate to Drain "Miller" Charge |   |  | 2.5 |    | nC |

### Drain-Source Diode Characteristics

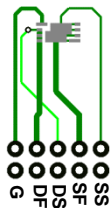
|          |                                       |   |  |     |     |    |
|----------|---------------------------------------|---|--|-----|-----|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}$ , $I_S = 7\text{ A}$ (Note 2)     |  | 0.8 | 1.2 | V  |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ |  | 43  | 70  | ns |
| $Q_{rr}$ | Reverse Recovery Charge               |   |  | 44  | 71  | nC |

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 60  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 160  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.
- $E_{AS}$  of 121 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 30\text{ A}$ .
- Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

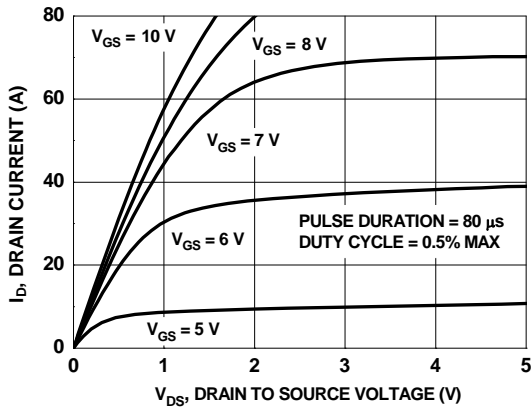


Figure 1. On-Region Characteristics

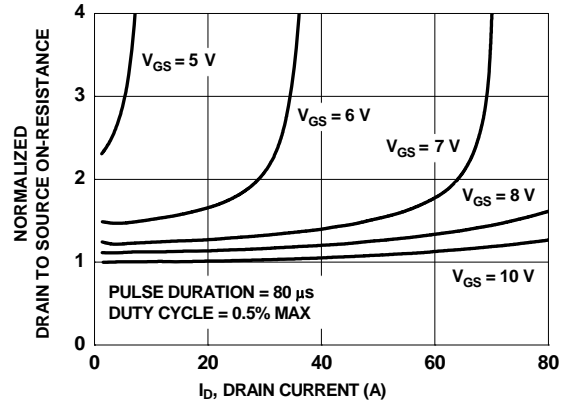


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

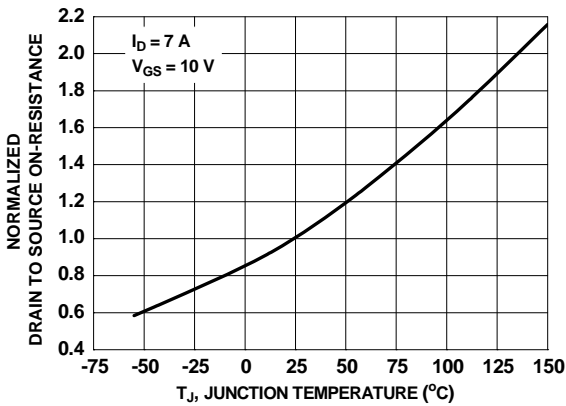


Figure 3. Normalized On-Resistance vs Junction Temperature

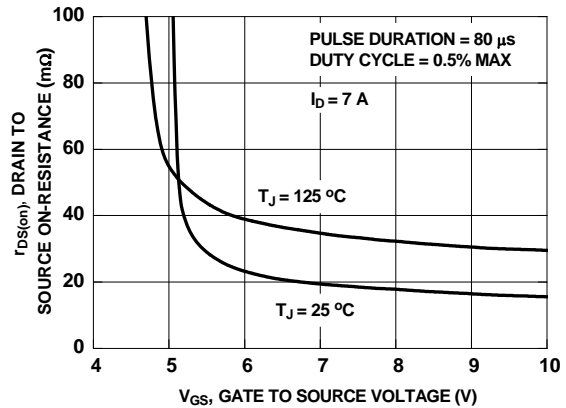


Figure 4. On-Resistance vs Gate to Source Voltage

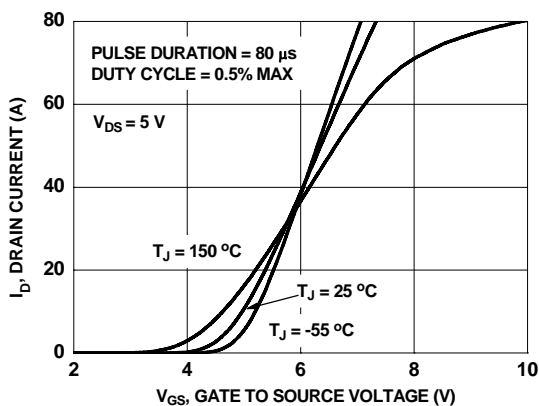


Figure 5. Transfer Characteristics

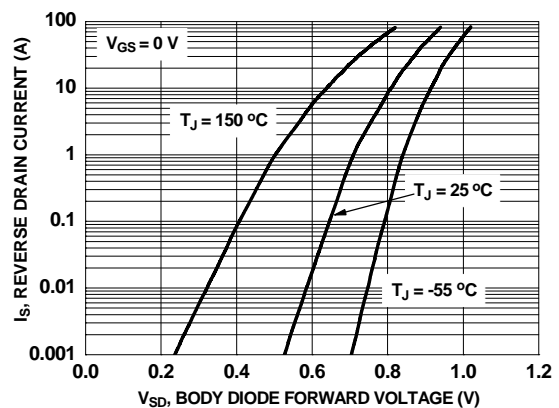
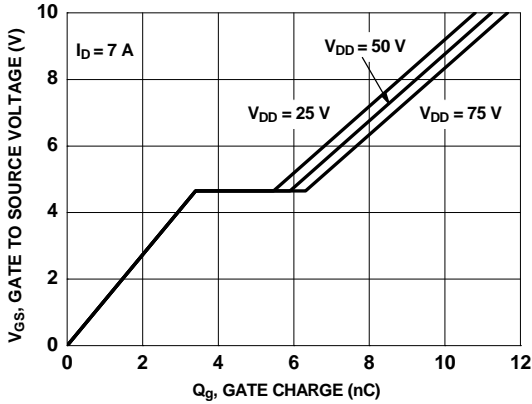
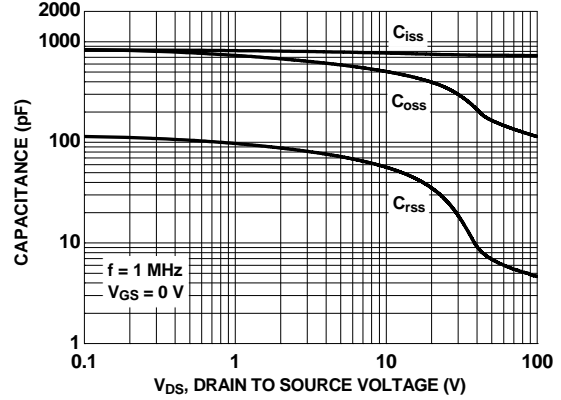


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

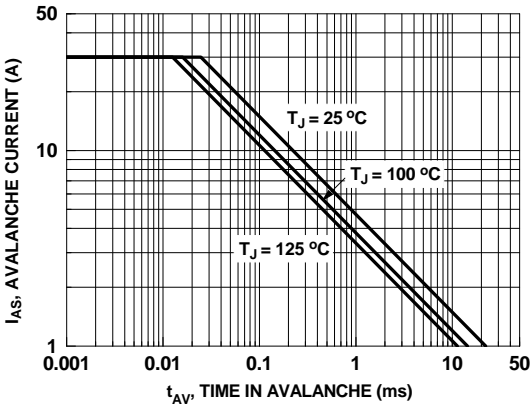
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



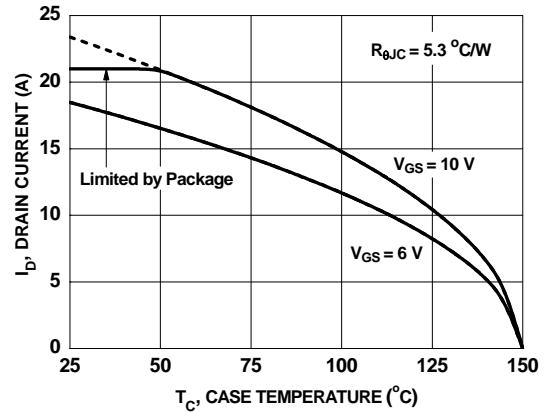
**Figure 7. Gate Charge Characteristics**



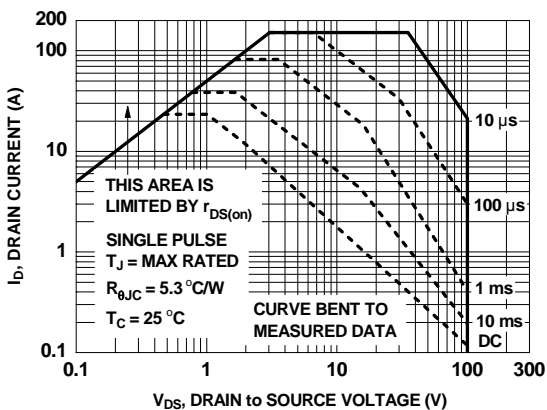
**Figure 8. Capacitance vs Drain to Source Voltage**



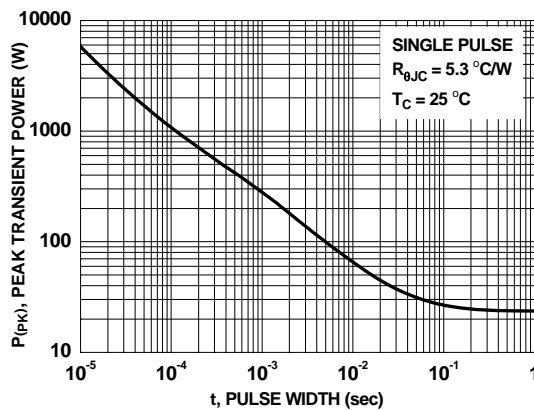
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

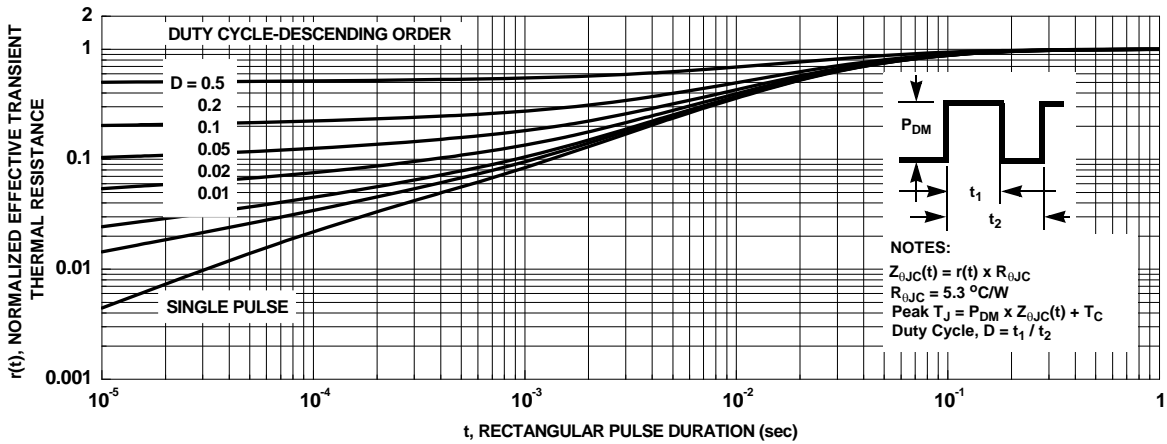


**Figure 11. Forward Bias Safe Operating Area**

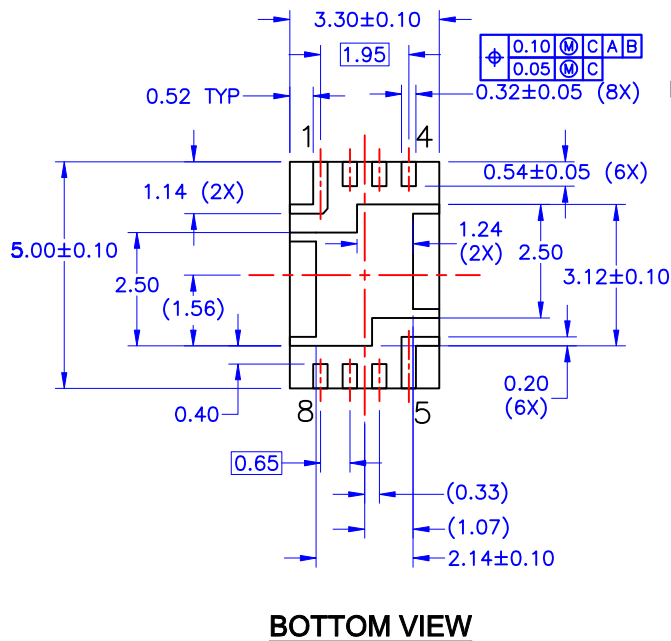
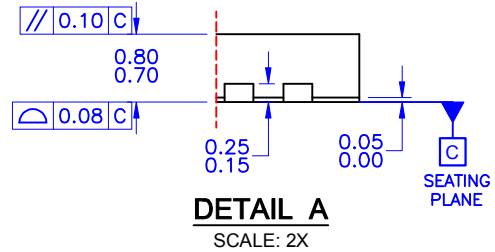
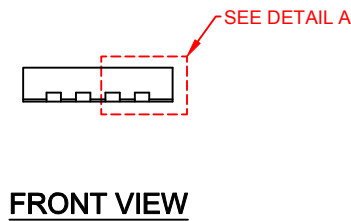
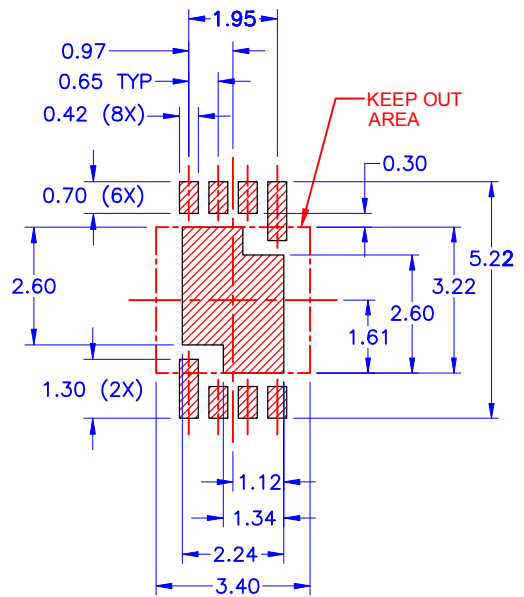
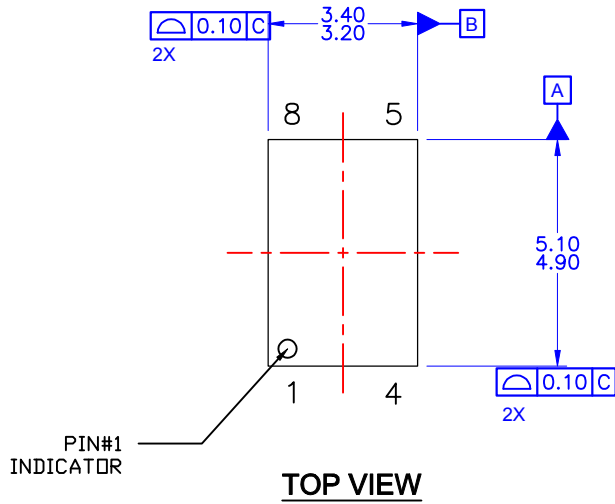


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO229 DATED 8/2012.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: MKT-PQFN08NREV1.

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