

COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _C = +25°C
Q1	30V	21mΩ @ V _{GS} = 10V	14A
		32mΩ @ V _{GS} = 4.5V	14A
Q2	-30V	39mΩ @ V _{GS} = -10V	-14A
		53mΩ @ V _{GS} = -4.5V	-14A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

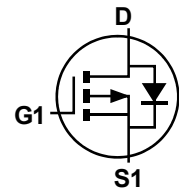
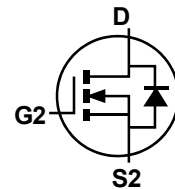
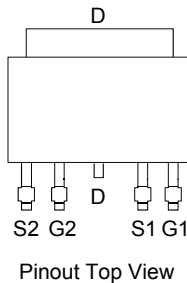
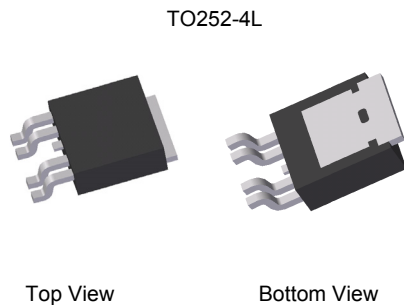
- Motor Control
- Power Management Functions
- DC-DC Converters
- Backlighting

Features and Benefits

- 0.6mm Profile – Ideal for Low Profile Applications
- PCB Footprint of 4mm²
- Low Gate Threshold Voltage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: TO252-4
- Case Material: Molded Plastic, "Green" Molding Compound UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish – Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 **e3**
- Weight: 0.027 grams (approximate)



Ordering Information (Note 4)

Part Number	Case	Packaging
DMC3021LK4-13	TO252-4	2500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

Marking Information



- ☺ = Manufacturer's Marking
- C3021L = Product Type Marking Code
- YYWW = Date Code Marking
- YY = Year (ex: 11 = 2011)
- WW = Week (01 - 53)

Maximum Ratings N-CHANNEL – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C	I _D	9.4	A
		T _A = +70°C		7.5	
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _C = +25°C	I _D	14	A
		T _C = +70°C		14	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	70	A
Avalanche Current, (Notes 7) L = 0.1mH			I _{AS}	16	A
Avalanche Energy, (Notes 7) L = 0.1mH			E _{AS}	13	mJ

Maximum Ratings P-CHANNEL – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V _{DSS}	-30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = -10V	Steady State	T _A = +25°C	I _D	-6.8	A
		T _A = +70°C		-5.3	
Continuous Drain Current (Note 6) V _{GS} = -10V	Steady State	T _C = +25°C	I _D	-14	A
		T _C = +70°C		-14	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	-50	A
Avalanche Current, (Notes 7) L = 0.1mH			I _{AS}	-16	A
Avalanche Energy, (Notes 7) L = 0.1mH			E _{AS}	13	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

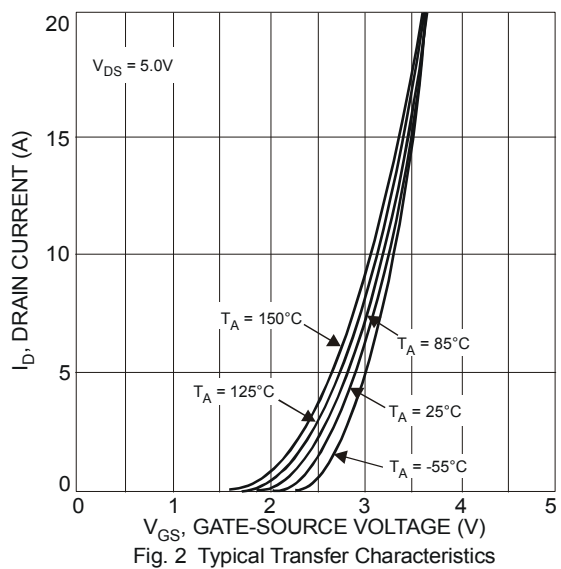
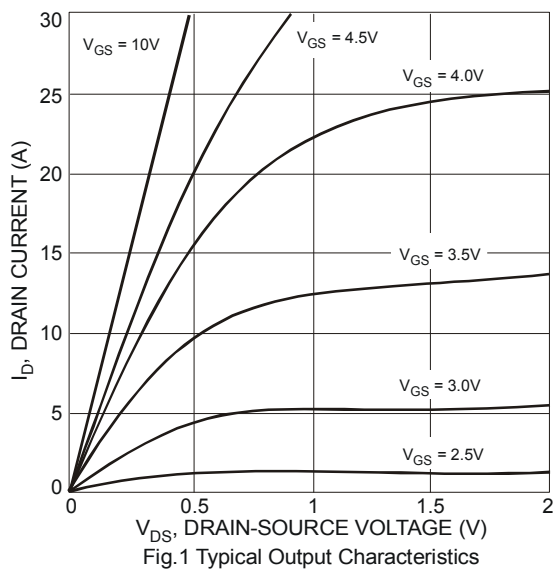
Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	2.7	W
	T _A = +70°C		1.7	
Total Power Dissipation (Note 6)	T _C = +25°C		22	
	T _C = +70°C		14	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	R _{θJA}	46	°C/W
Thermal Resistance, Junction to Case (Note 6)	Steady state	R _{θJC}	5.5	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

- Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate
 7. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = 25°C
 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing.

Electrical Characteristics N-CHANNEL – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current @T _C = +25°C	I _{DSS}	—	—	1.0	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	1	1.5	2.1	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	14	21	mΩ	V _{GS} = 10V, I _D = 7A
		—	18	32		V _{GS} = 4.5V, I _D = 5.6A
Forward Transfer Admittance	Y _{fs}	—	8.5	—	S	V _{DS} = 5V, I _D = 7A
Diode Forward Voltage	V _{SD}	—	0.7	1.0	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	751	—	pF	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	121	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	110	—	pF	
Gate Resistance	R _g	—	1.5	—	Ω	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (4.5V)	Q _g	—	9	—	nC	V _{GS} = 10V, V _{DS} = 15V, I _D = 6A
Total Gate Charge (10V)	Q _g	—	17.4	—	nC	
Gate-Source Charge	Q _{gs}	—	2.2	—	nC	
Gate-Drain Charge	Q _{gd}	—	3	—	nC	
Turn-On Delay Time	t _{D(on)}	—	2.5	—	ns	V _{DD} = 15V, V _{GS} = 10V, R _G = 6Ω, R _L = 1.8Ω, I _D = 6.7A
Turn-On Rise Time	t _r	—	6.6	—	ns	
Turn-Off Delay Time	t _{D(off)}	—	19.0	—	ns	
Turn-Off Fall Time	t _f	—	6.3	—	ns	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.



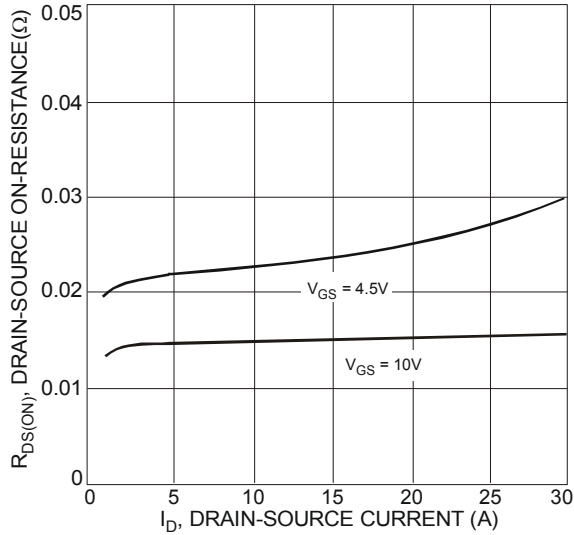


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

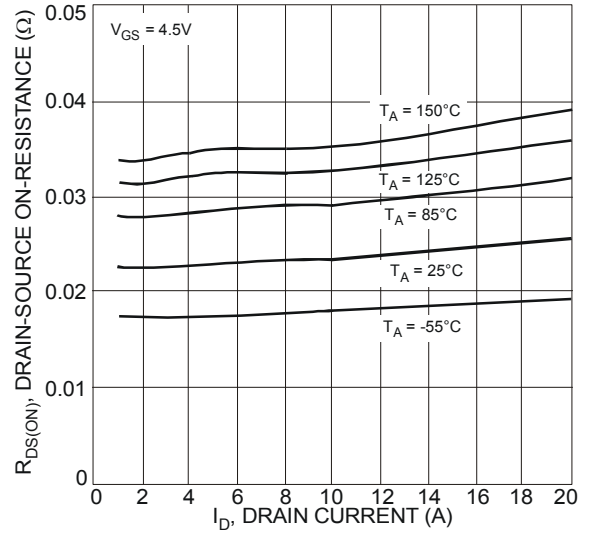


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

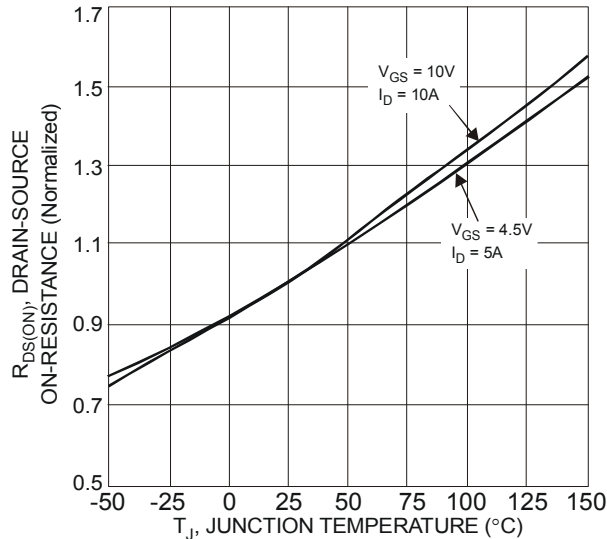


Fig. 5 On-Resistance Variation with Temperature

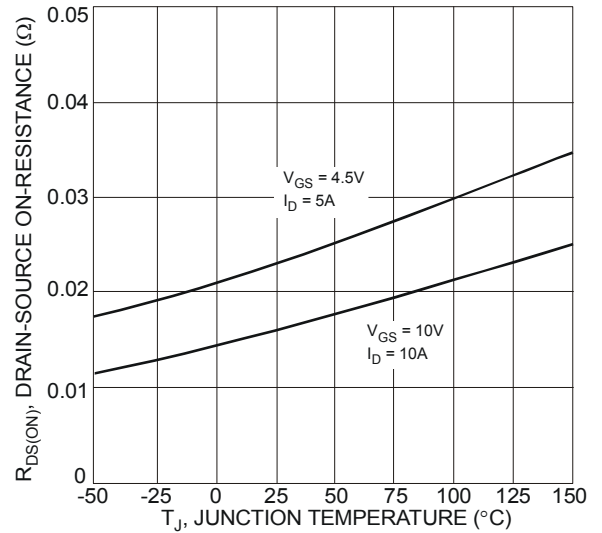


Fig. 6 On-Resistance Variation with Temperature

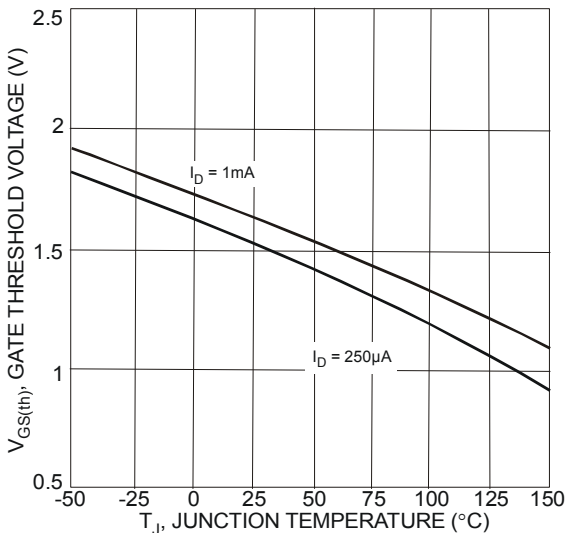


Fig. 7 On-Resistance Variation with Temperature

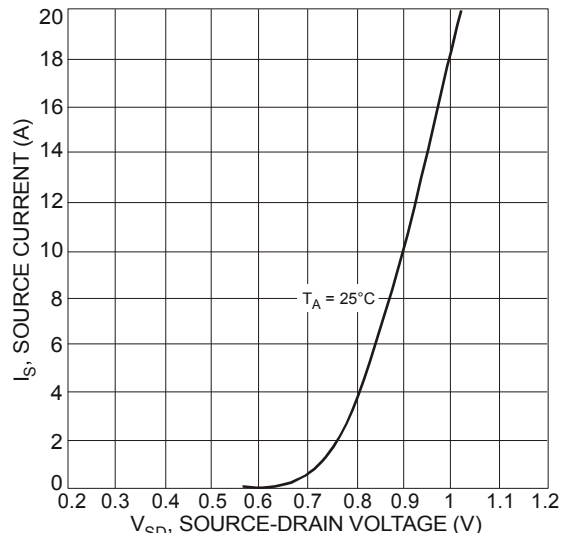


Fig. 8 Diode Forward Voltage vs. Current

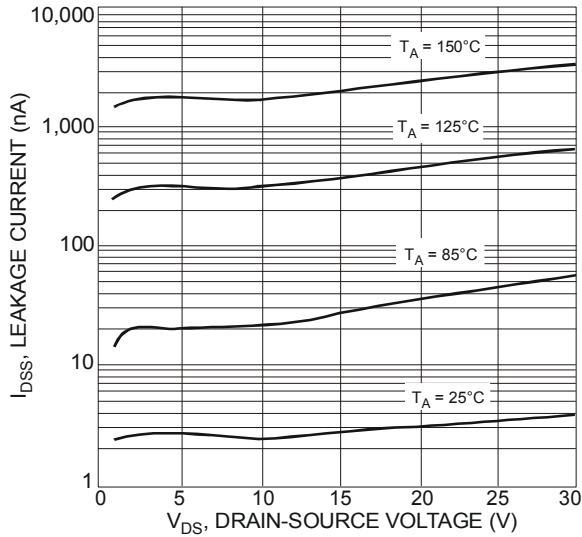


Fig. 9 Typical Drain-Source Leakage Current vs. Voltage

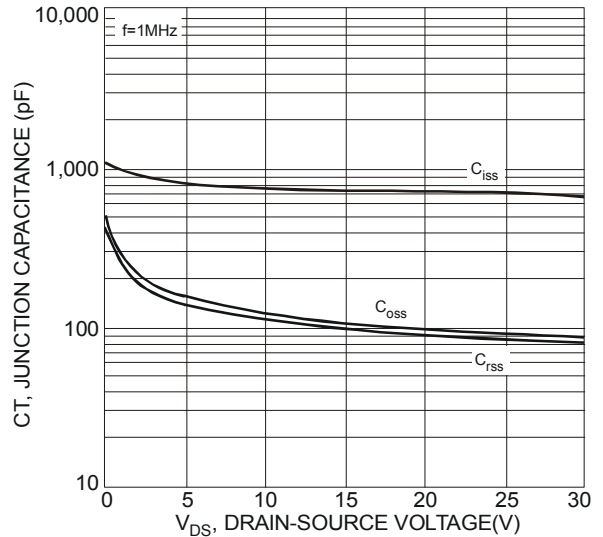


Fig. 10 Typical Junction Capacitance

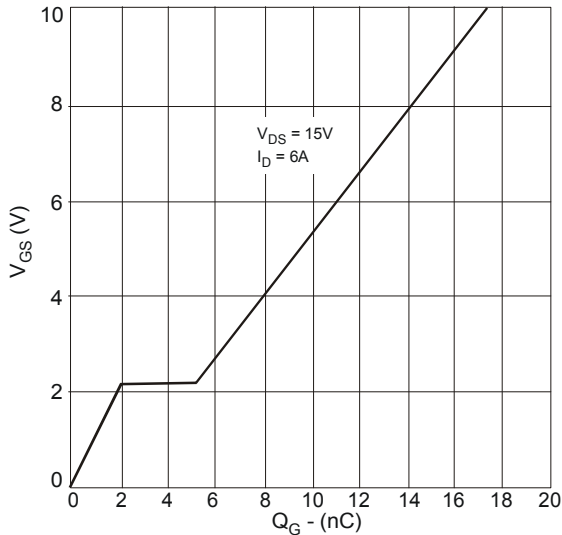


Fig. 11 Gate Charge Characteristics

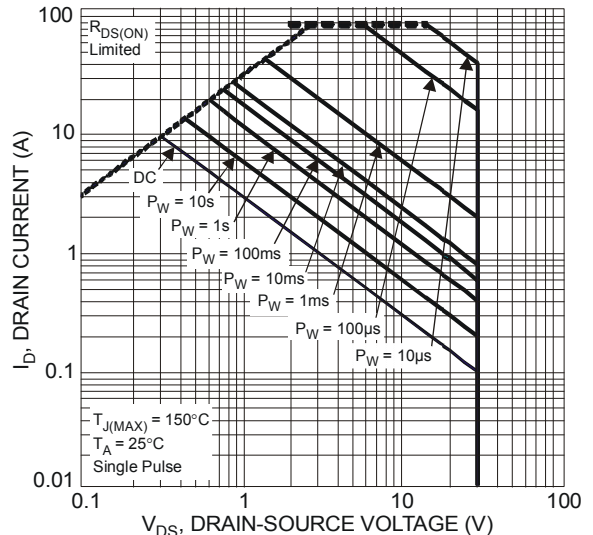
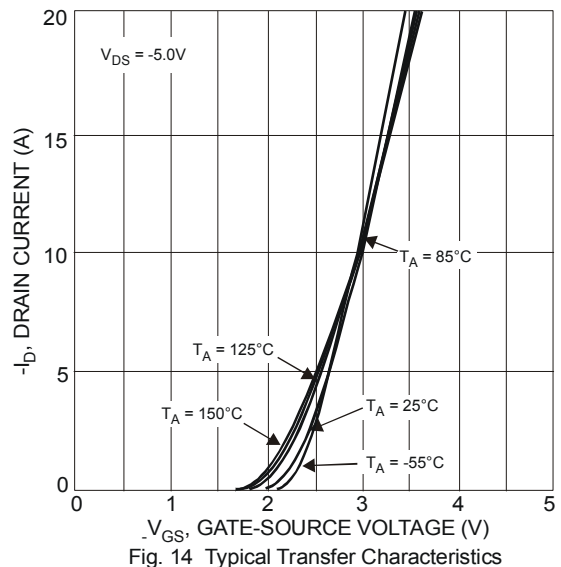
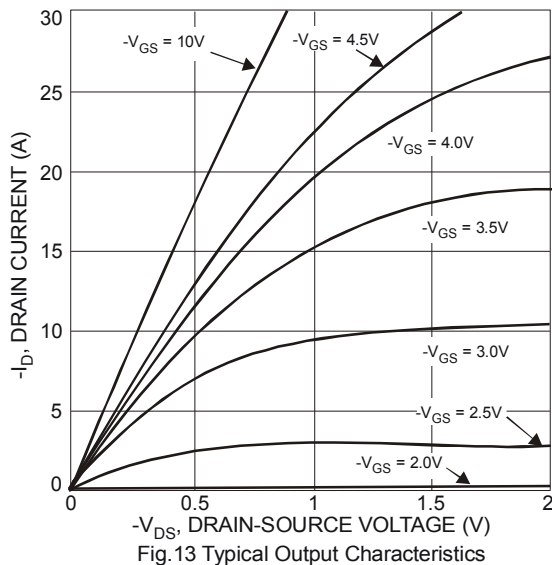


Fig. 12 SOA, Safe Operation Area

Electrical Characteristics P-CHANNEL – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current @T _C = +25°C	I _{DSS}	—	—	-1	μA	V _{DS} = -30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	-1	-1.7	-2.2	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	30	39	mΩ	V _{GS} = -10V, I _D = -4.3A
		—	42	53		V _{GS} = -4.5V, I _D = -3.7A
Forward Transfer Admittance	Y _{fs}	—	10	—	S	V _{DS} = -5V, I _D = -4.3A
Diode Forward Voltage	V _{SD}	—	-0.75	-1.0	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	1039	—	pF	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	144	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	134	—	pF	
Gate Resistance	R _g	—	13	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (4.5V)	Q _g	—	10.1	—	nC	V _{GS} = -10V, V _{DS} = -15V, I _D = -6A
Total Gate Charge (10V)	Q _g	—	21.1	—	nC	
Gate-Source Charge	Q _{gs}	—	2.8	—	nC	
Gate-Drain Charge	Q _{gd}	—	3.2	—	nC	
Turn-On Delay Time	t _{D(on)}	—	10.1	—	ns	V _{DS} = -15V, V _{GS} = -10V, R _G = 6Ω, I _D = -1A
Turn-On Rise Time	t _r	—	6.5	—	ns	
Turn-Off Delay Time	t _{D(off)}	—	50.1	—	ns	
Turn-Off Fall Time	t _f	—	22.2	—	ns	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.



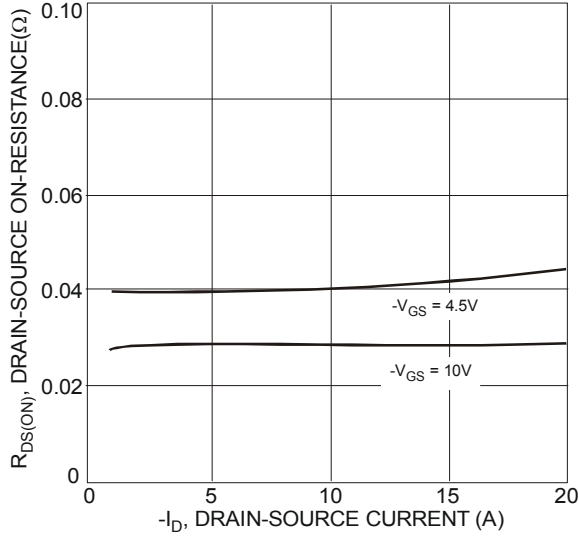


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

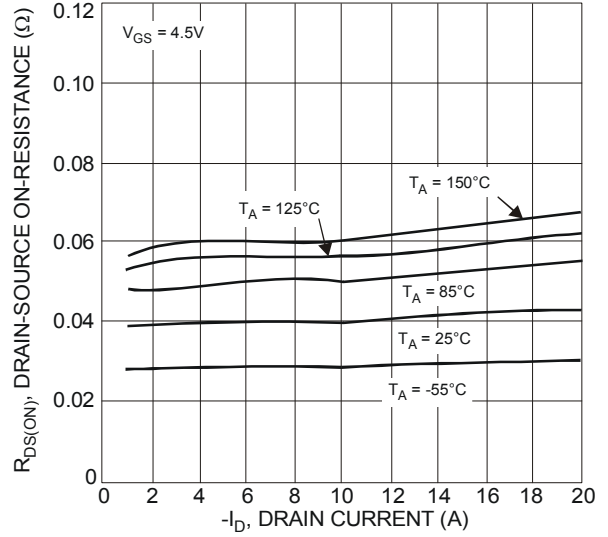


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

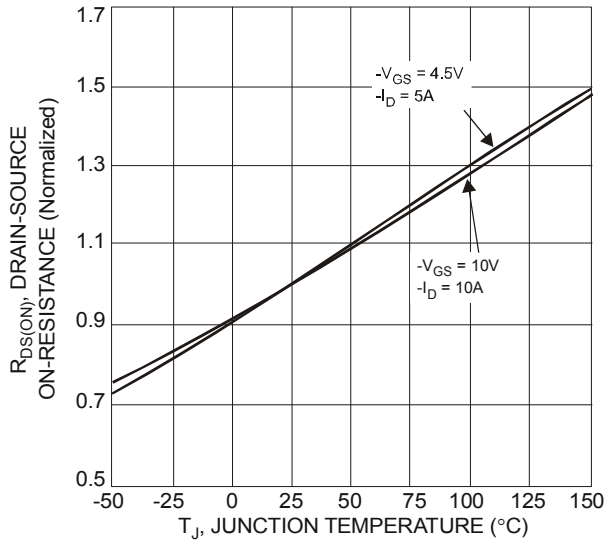


Fig. 17 On-Resistance Variation with Temperature

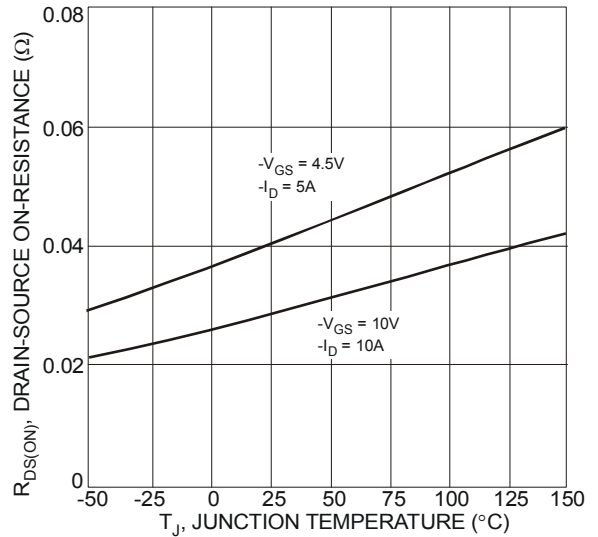


Fig. 18 On-Resistance Variation with Temperature

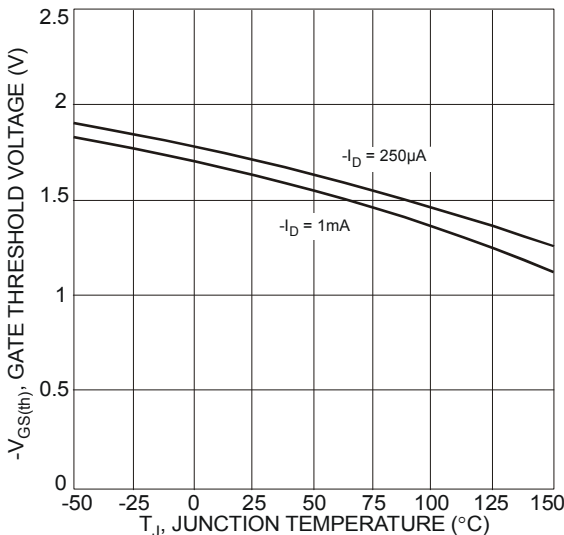


Fig. 19 On-Resistance Variation with Temperature

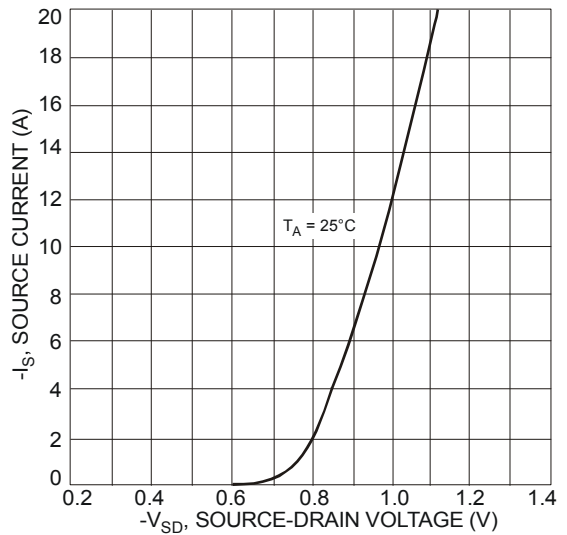


Fig. 20 Diode Forward Voltage vs. Current

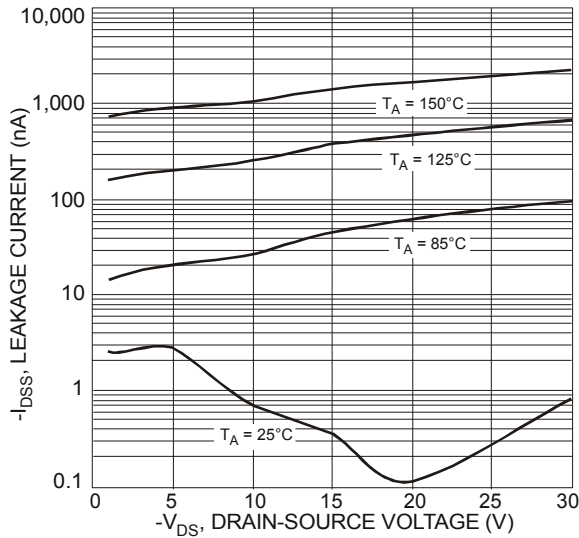


Fig. 21 Typical Drain-Source Leakage Current vs. Voltage

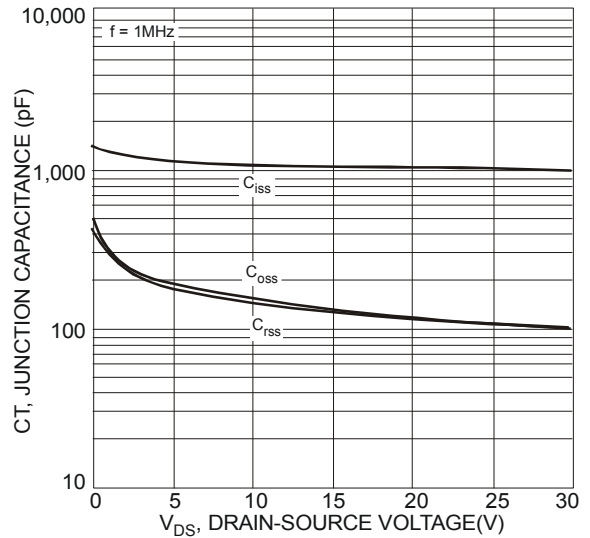


Fig. 22 Typical Junction Capacitance

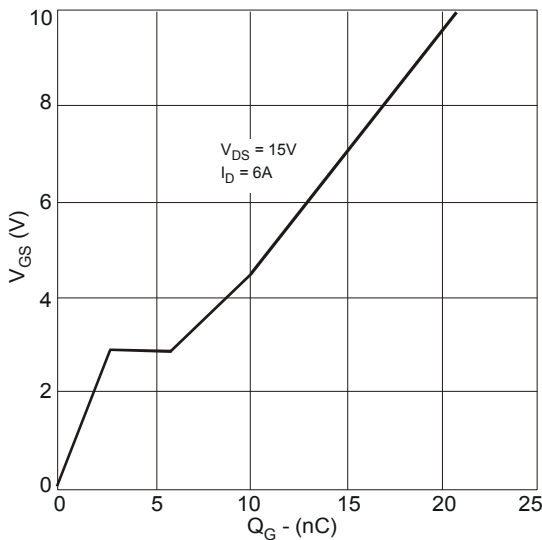


Fig. 23 Gate Charge Characteristics

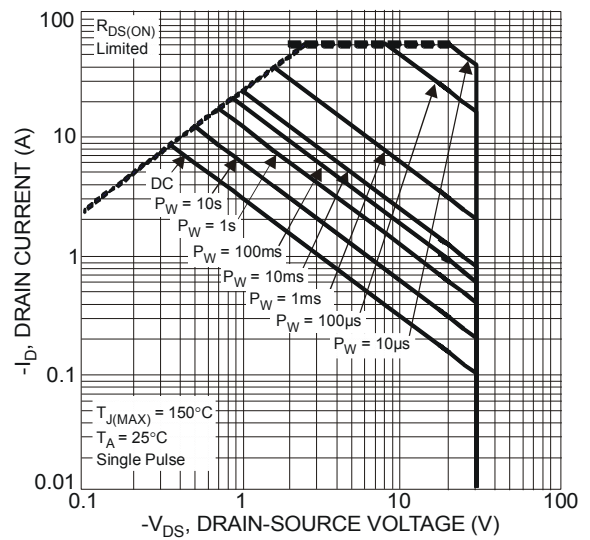


Fig. 24 SOA, Safe Operation Area

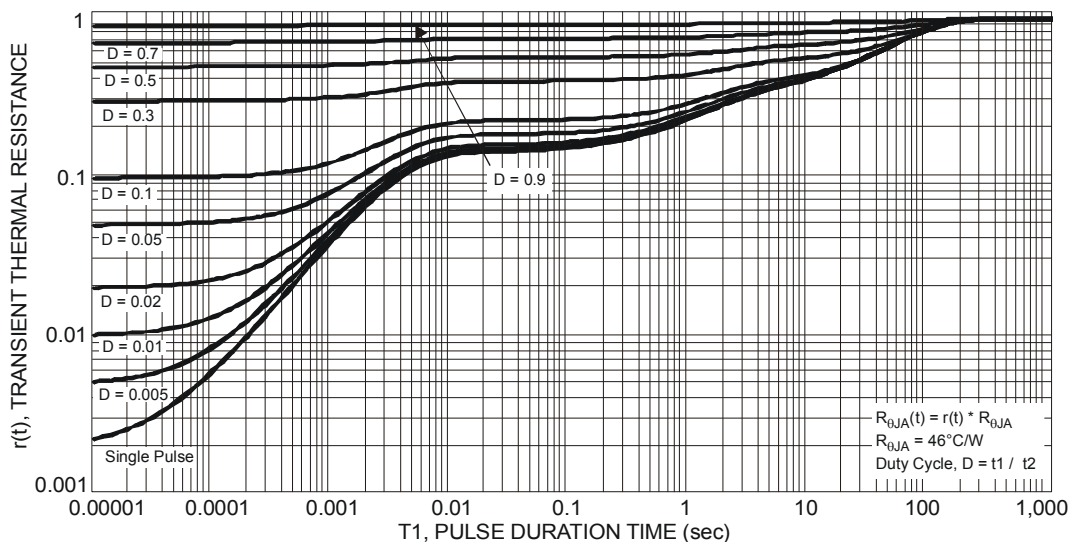
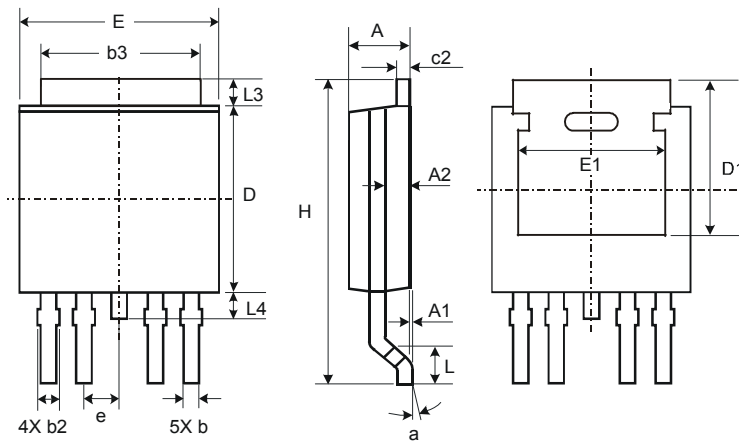


Fig. 25 Transient Thermal Resistance

Package Outline Dimensions

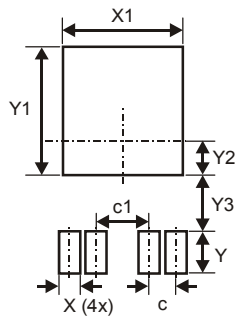
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



TO252-4			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.51	0.71	0.583
b1	0.61	0.79	0.70
b2	5.21	5.46	5.33
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	1.27
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
c	1.27
c1	2.54
X	1.00
X1	5.73
Y	2.00
Y1	6.17
Y2	1.64
Y3	2.66

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