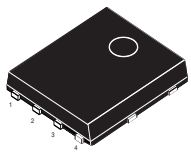
# STL40N75LF3

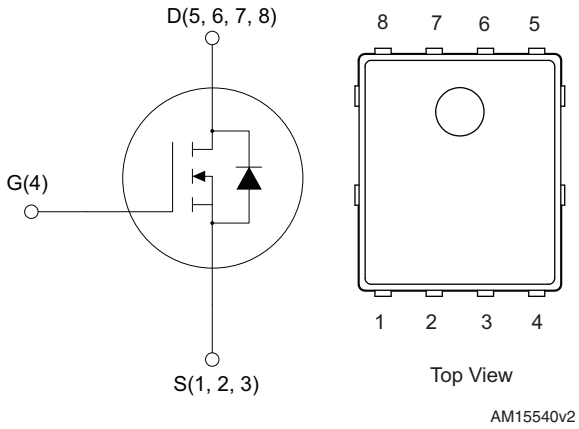
## N-channel 75 V, 16 mΩ typ., 10 A STripFET™ III Power MOSFET in a PowerFLAT™ 5x6 package

**Datasheet - production data**



**PowerFLAT™ 5x6**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DSS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STL40N75LF3 | 75 V | 19 mΩ | 10 A |

- N-channel enhancement mode
- Low gate charge
- Low threshold voltage device

## Applications

- Switching applications

## Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL40N75LF3 | 40N75LF3 | PowerFLAT™ 5x6 | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 75 | V |
| $V_{GS}$ | Gate-source voltage | +20\-16 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 40 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | 26 | A |
| $I_{DM}$ (1)(2) | Drain current (pulsed) | 160 | A |
| $I_D$ (3) | Drain current (continuous) at $T_{pcb}$ = 25 °C | 10 | A |
| $I_D$ (3) | Drain current (continuous) at $T_{pcb}$=100 °C | 6 | A |
| $P_{TOT}$ (1) | Total dissipation at $T_C$ = 25 °C | 75 | W |
| $P_{TOT}$ (3) | Total dissipation at $T_{pcb}$ = 25 °C | 4.8 | W |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -55 to 175 | °C |

1. The value is rated according to $R_{thj\text{-}case}$
2. Pulse width limited by safe operating area
3. The value is rated according to $R_{thj\text{-}pcb}$

**Table 3. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 2 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-ambient | 31.3 | °C/W |

1. When mounted on FR-4 board of 1 inch², 2oz Cu., t < 10 sec.

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified).

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS}$= 0) | $I_D$ = 250 µA | 75 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 75 V,<br>$V_{DS}$ = 75 V, $T_C$ = 125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = +20 / -16 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250 µA | 1 | | | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10 V, $I_D$= 20 A<br>$V_{GS}$= 5 V, $I_D$= 20 A | | 16<br>18.7 | 19<br>22 | mΩ<br>mΩ |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V, f = 1 MHz,<br>$V_{GS}$ = 0 | - | 1300<br>228<br>15 | - | pF<br>pF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$ = 37.5 V, $I_D$ = 40 A<br>$V_{GS}$ = 5 V<br>*(see Figure 14)* | - | 12<br>5<br>5.3 | - | nC<br>nC<br>nC |
| $R_G$ | Gate input resistance | f=1 MHz gate DC bias=0<br>Test signal level = 20 mV<br>open drain | - | 3.5 | - | Ω |

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$= 37.5 V, $I_D$= 20 A,<br>$R_G$= 4.7 Ω, $V_{GS}$=10 V<br>*(see Figure 13)* | - | 12<br>25<br>25<br>3 | - | ns<br>ns<br>ns<br>ns |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 40 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | | | 160 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 40 A, $V_{GS}$=0 | - | | 1.1 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 40 A,<br>di/dt = 100 A/µs,<br>$V_{DD}$=60 V | - | 35<br>44<br>27 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

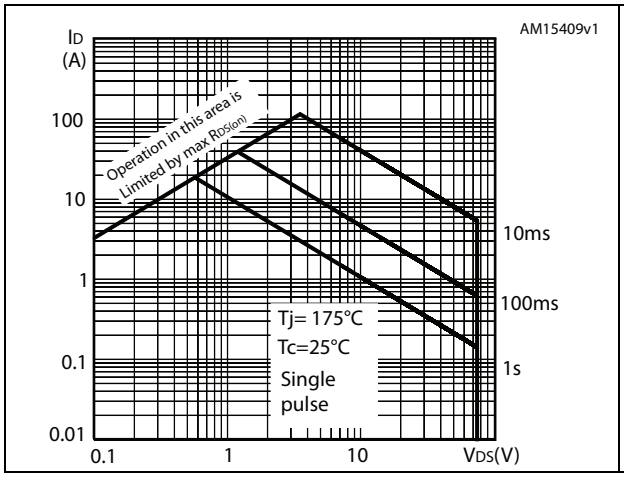



**Figure 3. Thermal impedance**

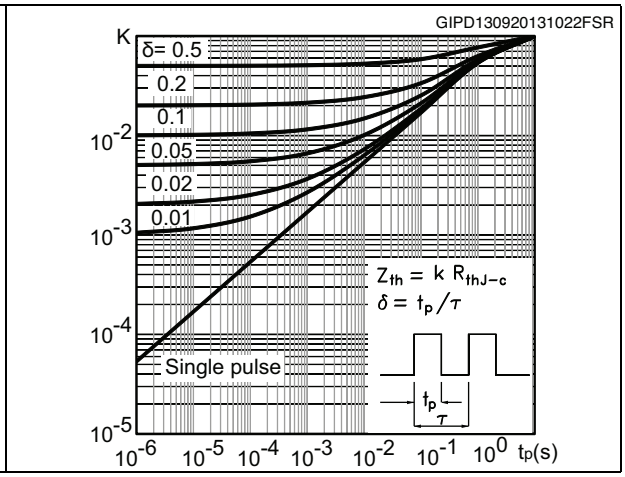



**Figure 4. Output characteristics**

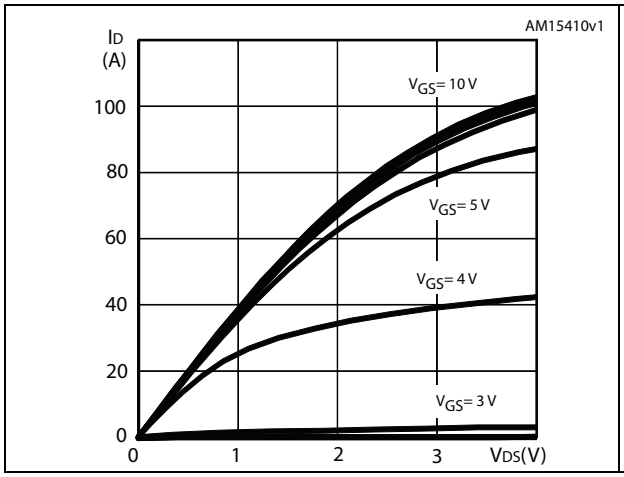



**Figure 5. Transfer characteristics**

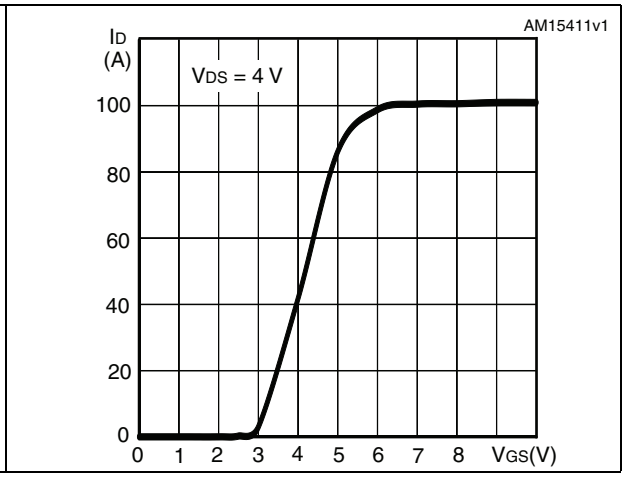



**Figure 6. Gate charge vs gate-source voltage**

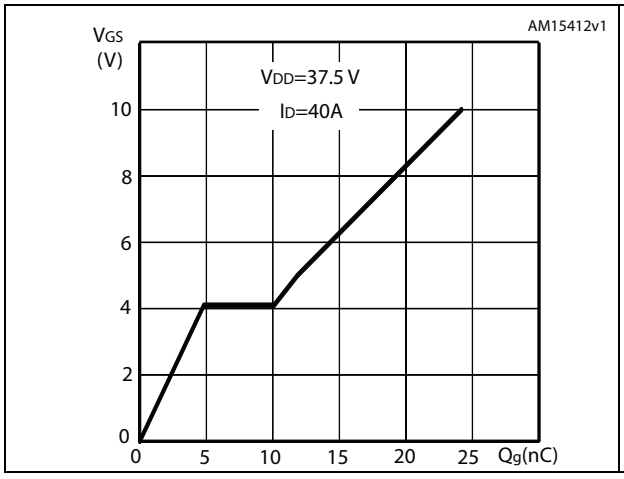



**Figure 7. Static drain-source on-resistance**

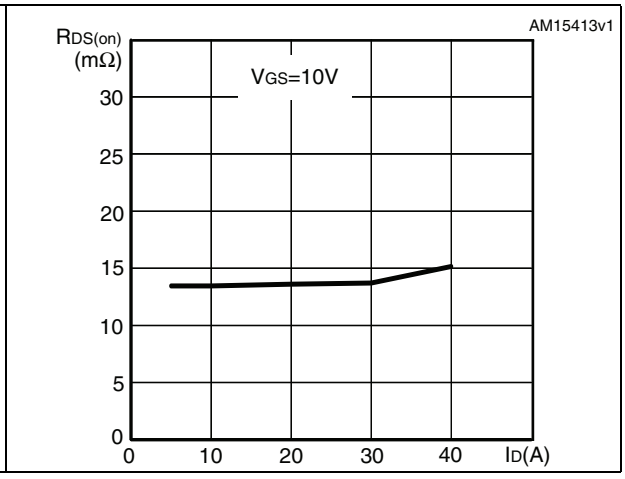


**Figure 8. Capacitance variations**

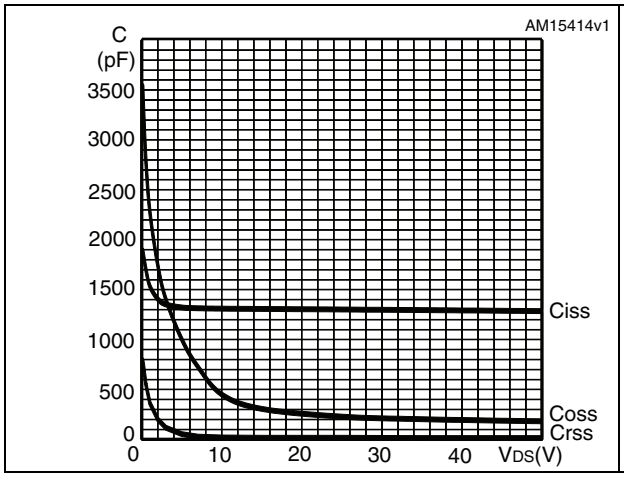



**Figure 9. Normalized $V(BR)_{DSS}$ vs temperature**

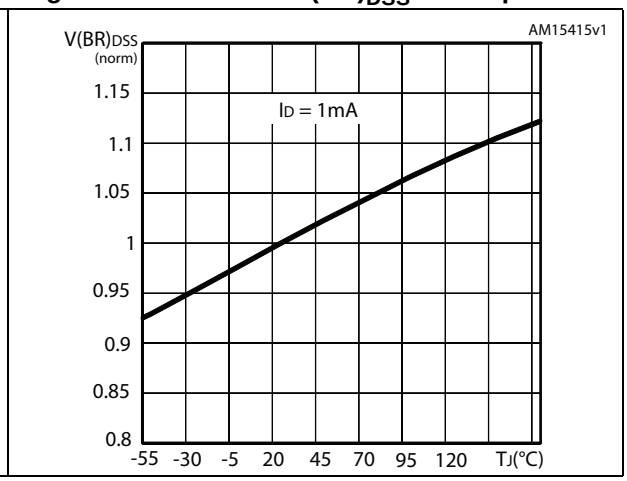



**Figure 10. Normalized gate threshold voltage vs temperature**

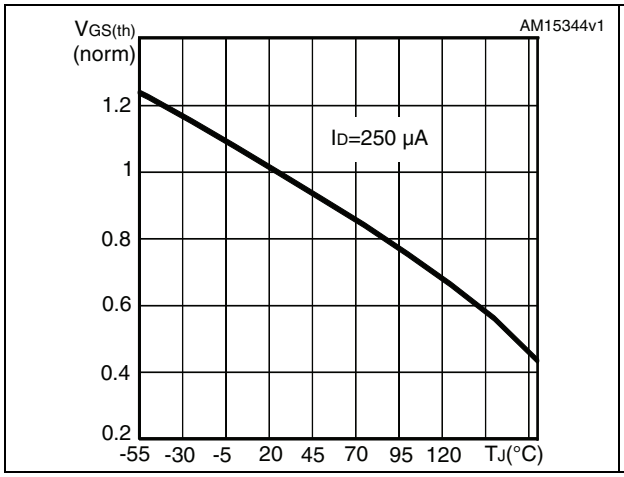



**Figure 11. Normalized on-resistance vs temperature**

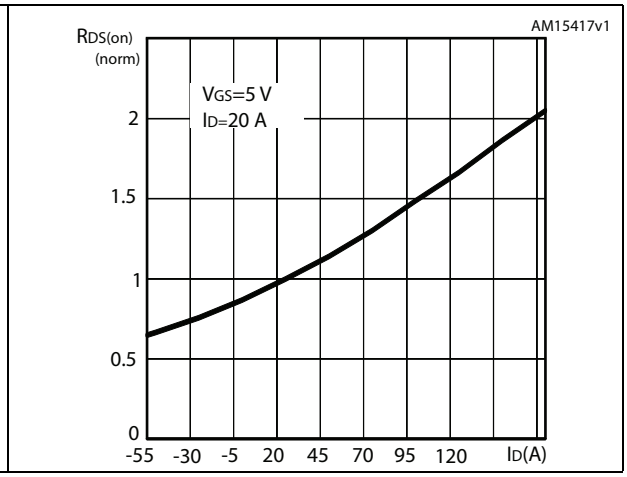
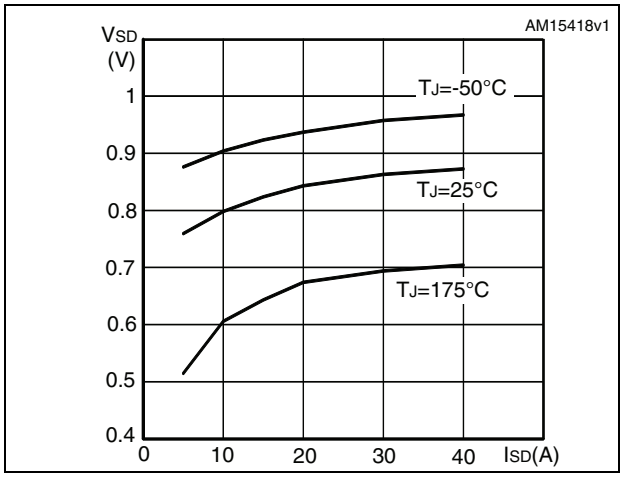



**Figure 12. Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

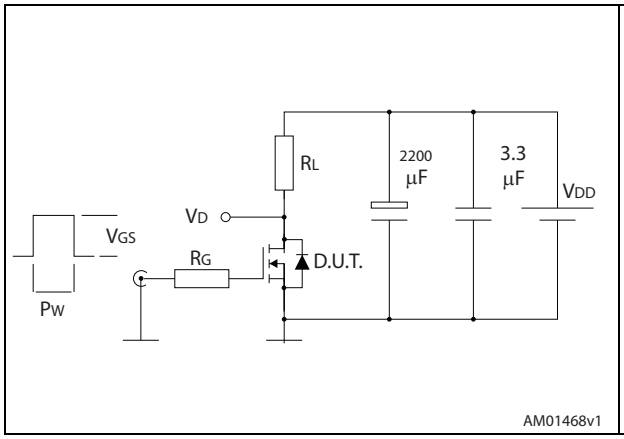



**Figure 14. Gate charge test circuit**

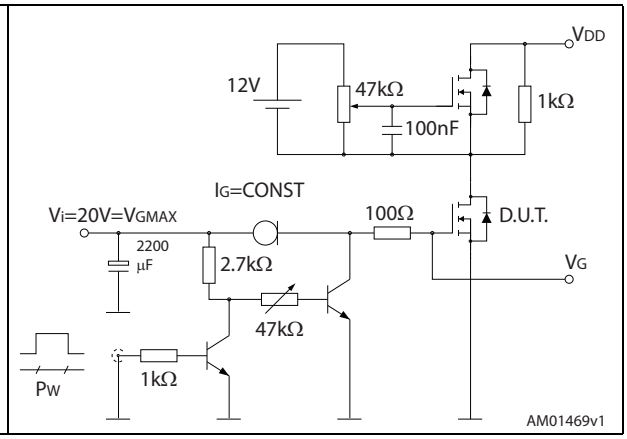



**Figure 15. Test circuit for inductive load switching and diode recovery times**

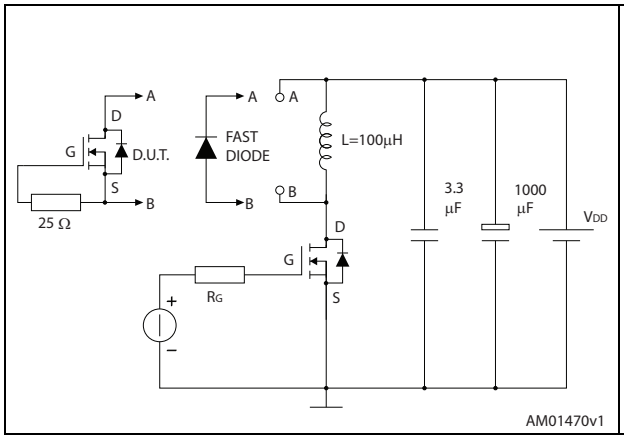



**Figure 16. Unclamped inductive load test circuit**

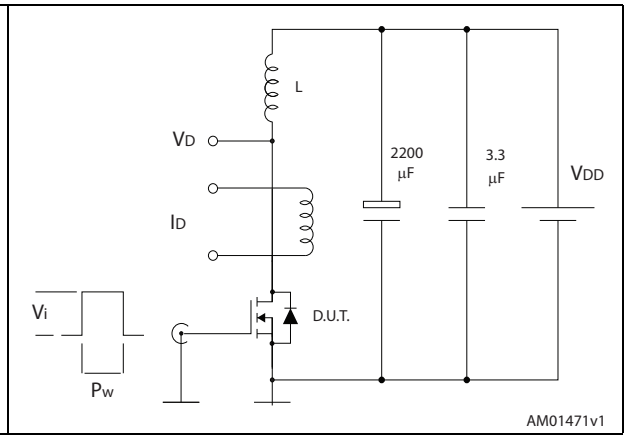



**Figure 17. Unclamped inductive waveform**

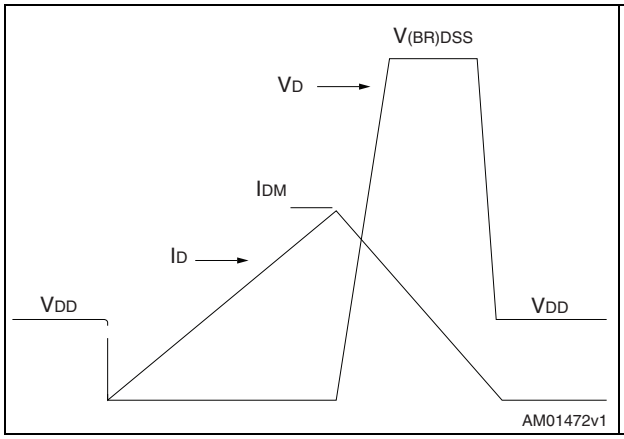
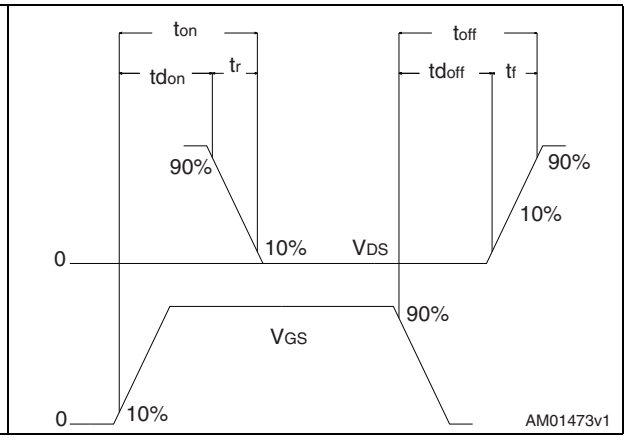



**Figure 18. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 19. PowerFLAT™ 5x6 type S-C drawings**

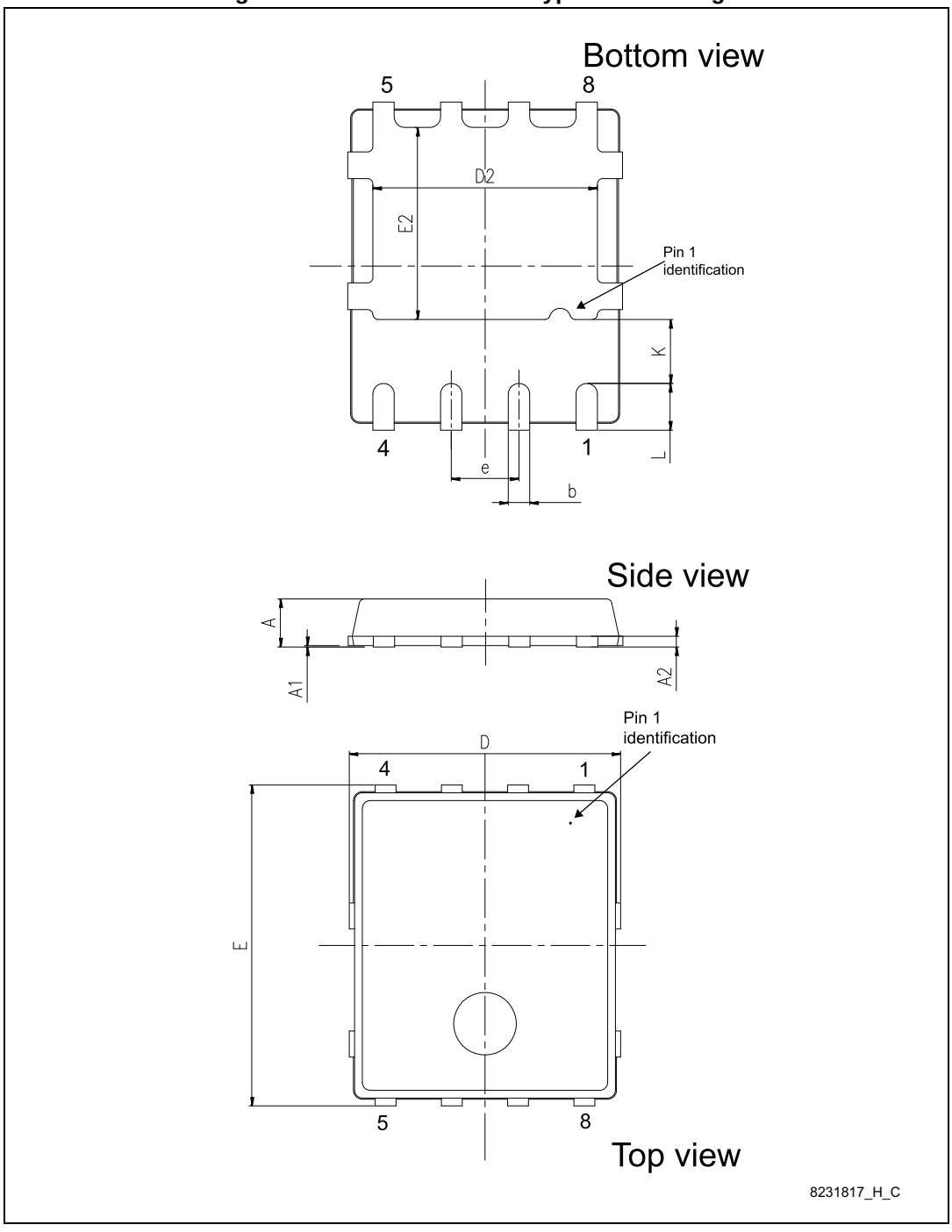
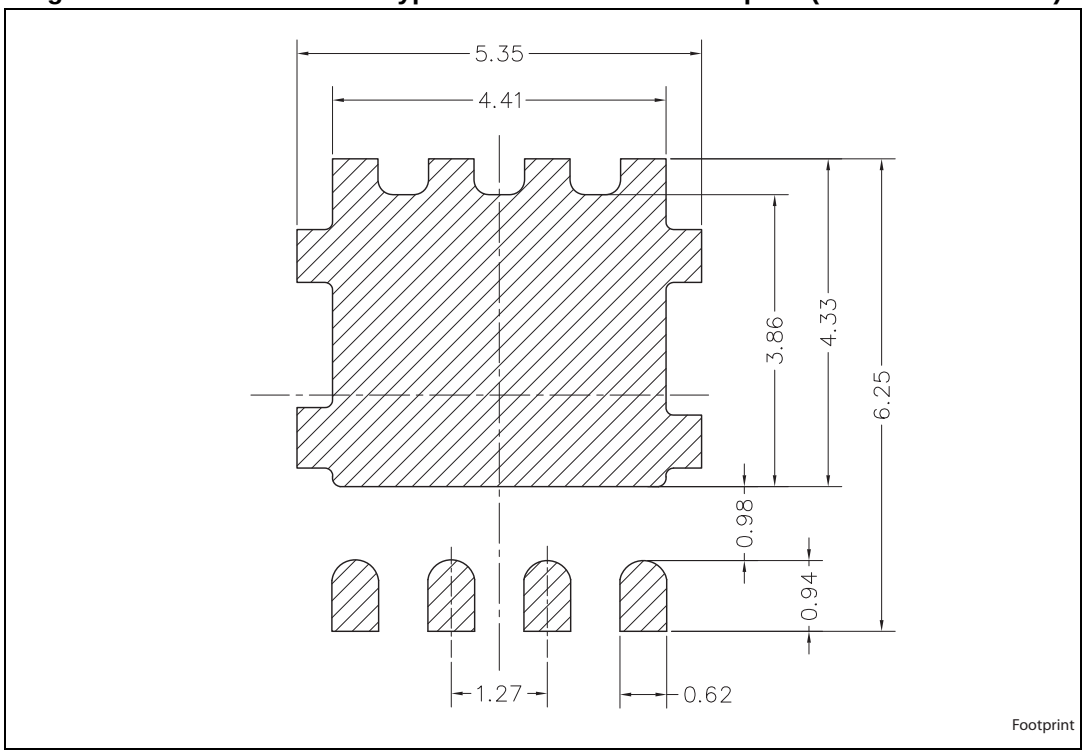


**Table 8. PowerFLAT™ 5x6 type S-C mechanical data**

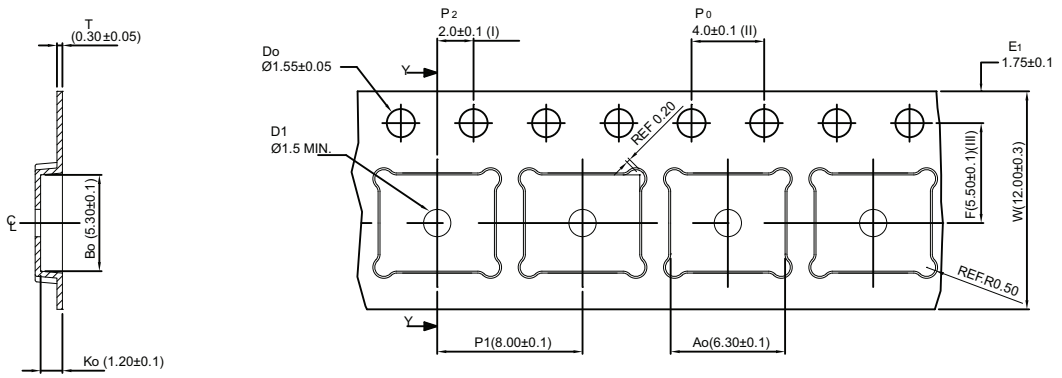
| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | | 5.20 | |
| E | | 6.15 | |
| D2 | 4.11 | | 4.31 |
| E2 | 3.50 | | 3.70 |
| e | | 1.27 | |
| e1 | | 0.65 | |
| L | 0.715 | | 1.015 |
| K | 1.05 | | 1.35 |

**Figure 20. PowerFLAT™ 5x6 type S-C recommended footprint (dimensions in mm)**



# 5 Packaging information

**Figure 21. PowerFLAT™ 5x6 type S-C tape**




(I) Measured from centerline of sprocket hole to centerline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centerline of sprocket hole to centerline of pocket.

Base and bulk quantity 3000 pcs

8234350_Tape_rev_C

**Figure 22. PowerFLAT™ 5x6 type S-C package orientation in carrier tape**

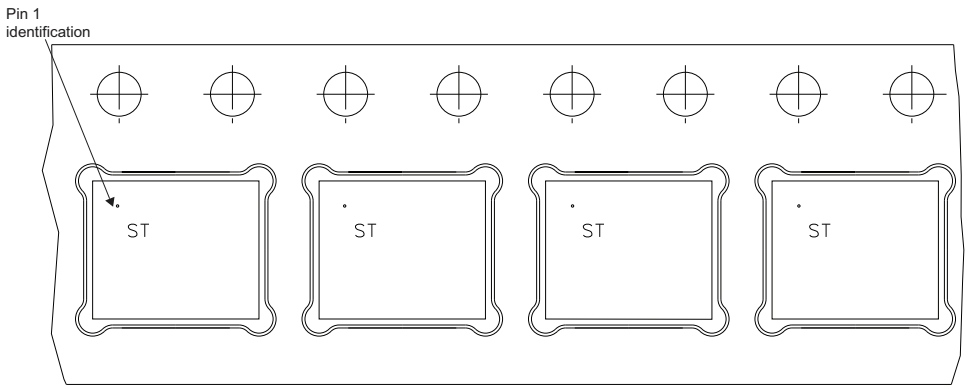
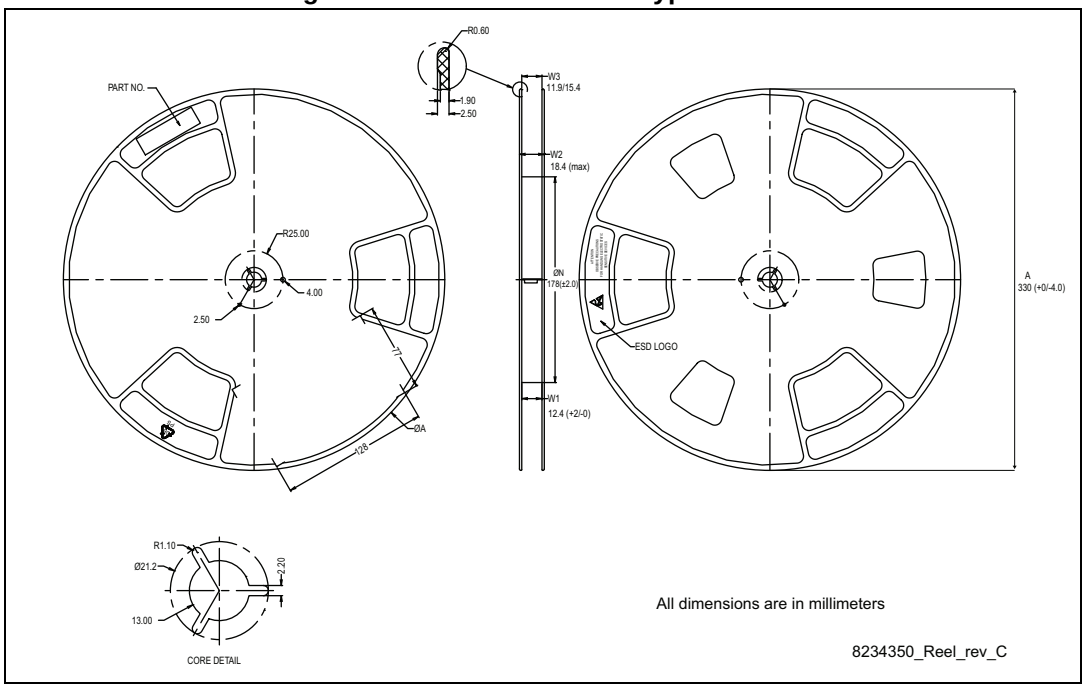


**Figure 23. PowerFLAT™ 5x6 type S-C reel**



# 6 Revision history

**Table 9. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 19-Oct-2012 | 1 | First release. |
| 24-Feb-2014 | 2 | Deleted note in the table of *Features*.<br>Updated *Figure 1*.<br>Updated values of $P_{TOT}$ , $T_J$ and $T_{stg}$ in *Table 2*.<br>Updated notes in *Table 2*.<br>Updated $V_{GS}$ test condition in*Table 5*.<br>Updated $V_{DD}$ test condition in*Table 6*.<br>Removed $T_j$ test condition from *Table 7*.<br>Updated *Figure 2*, *Figure 4*, *Figure 6*, *Figure 9* and *Figure 11*.<br>Updated mechanical data. |

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