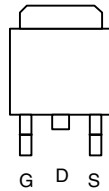


## N-Channel 75 V (D-S) MOSFET

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
75	0.007 at V <sub>GS</sub> = 10 V	110 <sup>d</sup>	69

**TO-263**


Top View

**Ordering Information:** SUM110N08-07P-E3 (Lead (Pb)-free)

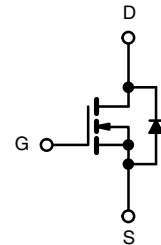
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFETS
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

### APPLICATIONS

- Synchronous Rectification



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	75	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	110 <sup>d</sup>
		T <sub>C</sub> = 70 °C	103
Pulsed Drain Current	I <sub>DM</sub>	180	A
Avalanche Current	I <sub>AS</sub>	50	
Single Avalanche Energy <sup>a</sup>	E <sub>AS</sub>	125	mJ
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	208.3 <sup>b</sup>
		T <sub>A</sub> = 25 °C <sup>c</sup>	3.75
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.6	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.

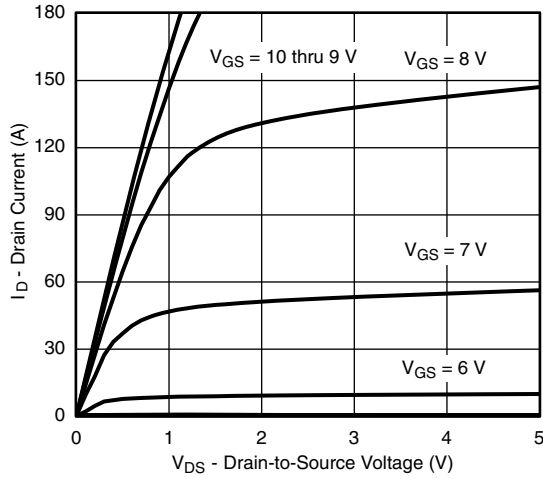
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	75			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 250$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	70			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0057	0.0070	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.0092	0.0112	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		43		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$		4250		$\mu\text{F}$
Output Capacitance	$C_{oss}$			580		
Reverse Transfer Capacitance	$C_{rss}$			230		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		69	105	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			23		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			21		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		1.2	2.4	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		17	30	ns
Rise Time <sup>c</sup>	$t_r$			5	10	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			22	40	
Fall Time <sup>c</sup>	$t_f$			6	15	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25\text{ }^\circ\text{C}$ <sup>b</sup>						
Continuous Current	$I_S$				110	A
Pulsed Current	$I_{SM}$				180	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 20\text{ A}, V_{GS} = 0\text{ V}$		0.83	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 75\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		65	100	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			2.5	5	A
Reverse Recovery Charge	$Q_{rr}$				85	150

## Notes:

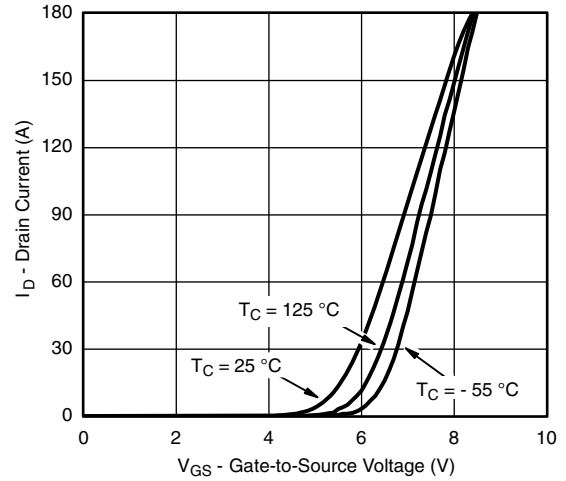
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

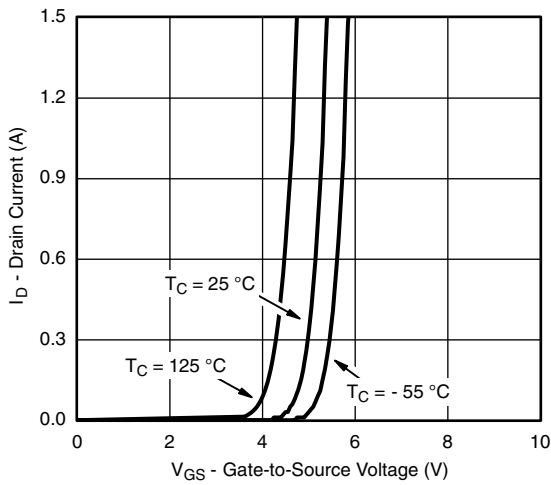
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



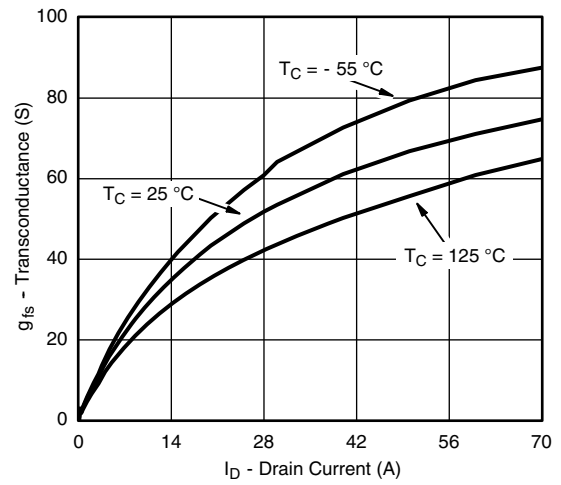
**Output Characteristics**



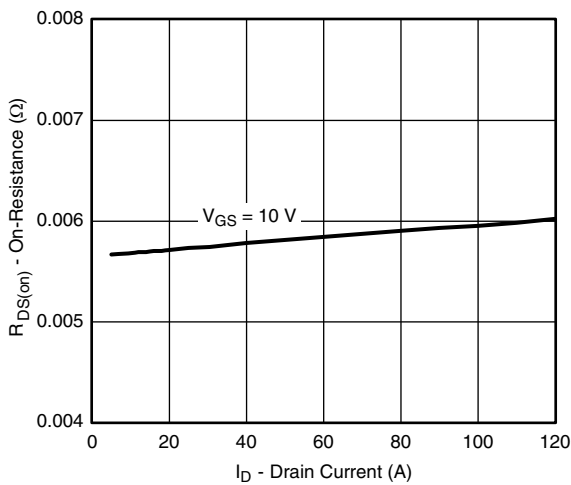
**Transfer Characteristics**



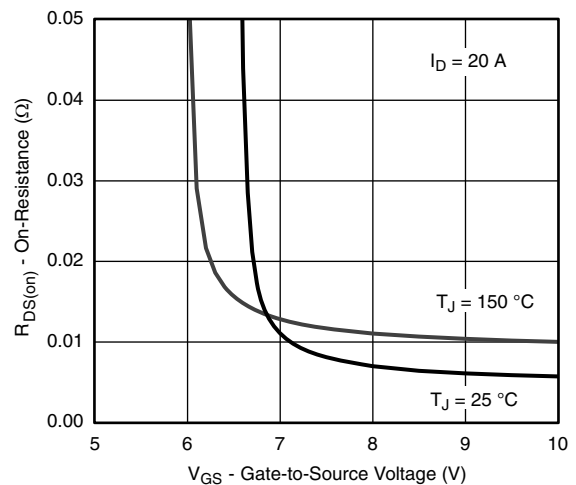
**Transfer Characteristics**



**Transconductance**

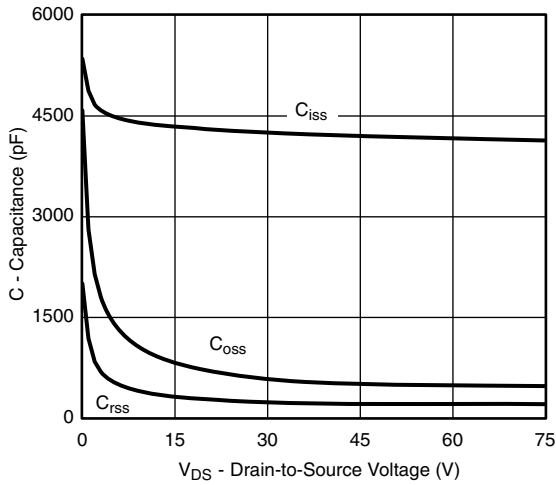


**On-Resistance vs. Drain Current**

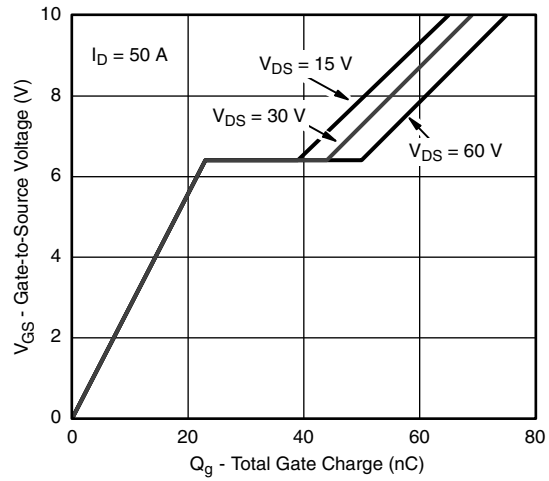


**On-Resistance vs. Gate-to-Source Voltage**

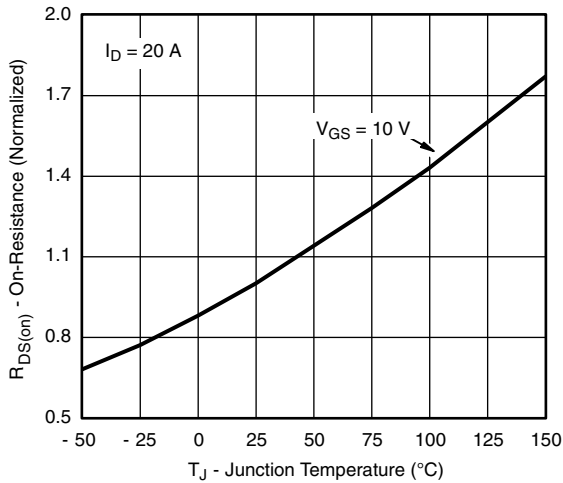
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



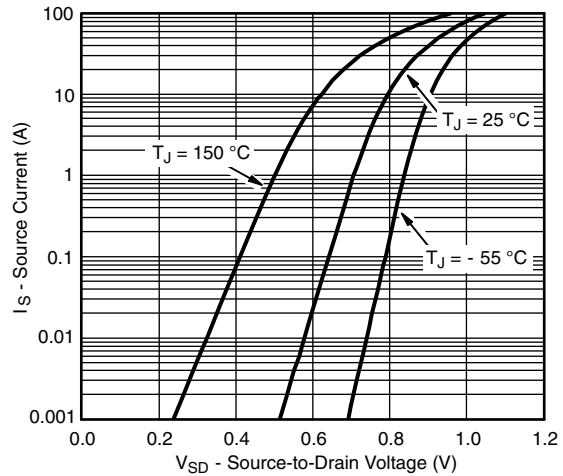
**Capacitance**



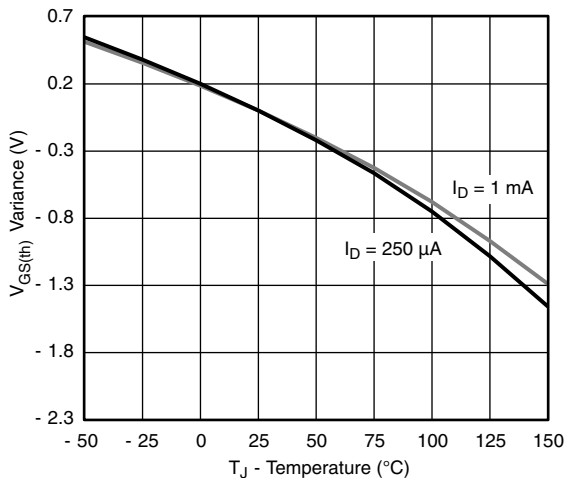
**Gate Charge**



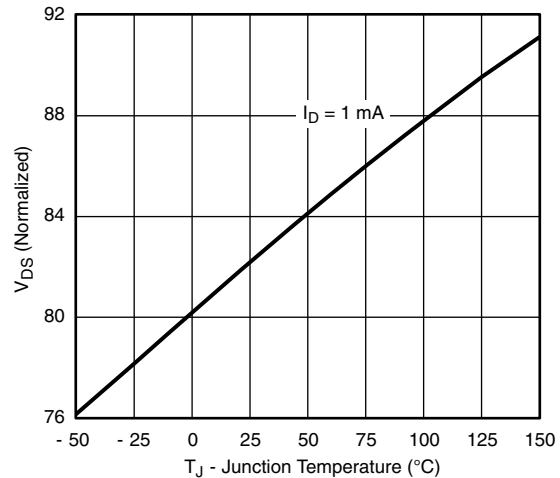
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**

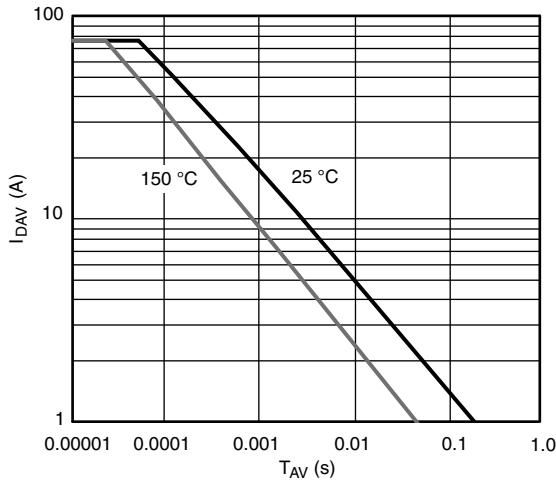


**Threshold Voltage**

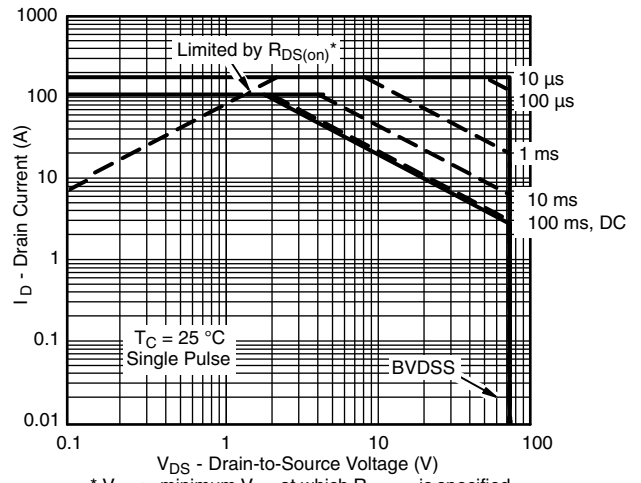


**Drain Source Breakdown vs. Junction Temperature**

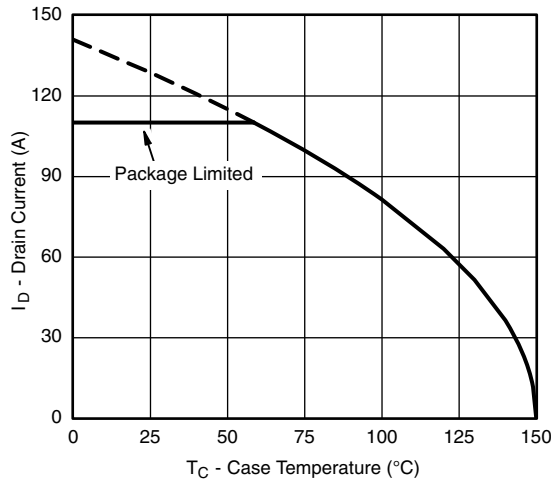
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Single Pulse Avalanche Current Capability vs. Time**

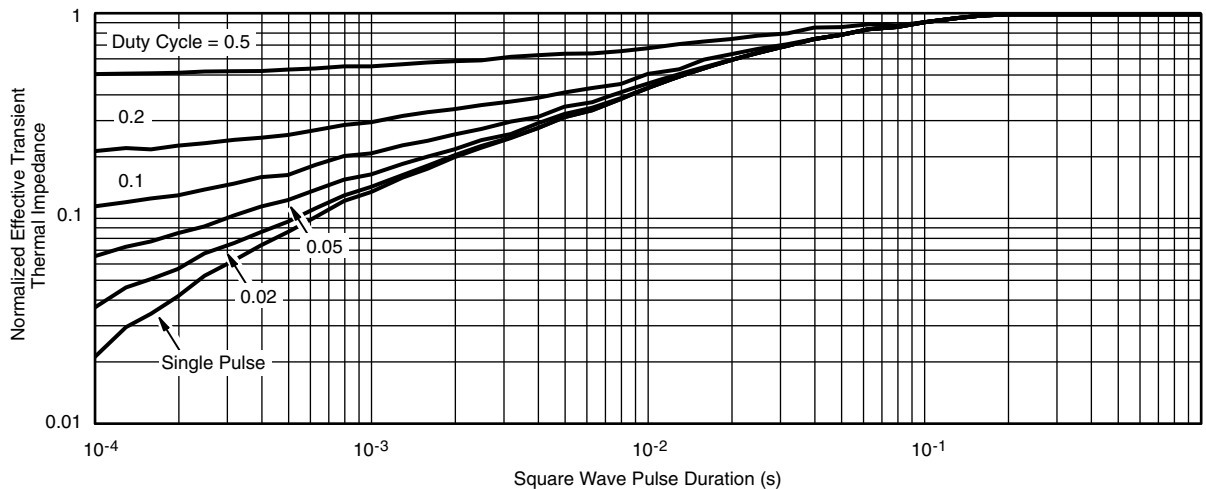


**Safe Operating Area, Junction-to-Case**  
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**Current Derating\*, Junction-to-Case**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**Normalized Thermal Transient Impedance, Junction-to-Case**

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