

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

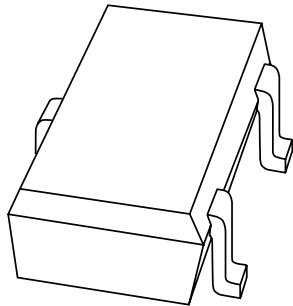
- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via salesaddresses@nexperia.com). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

DATA SHEET



PMSS3904 NPN switching transistor

Product data sheet
Supersedes data of 1997 Sep 03

1999 May 27

NPN switching transistor

PMSS3904

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- General purpose switching and amplification
- Telephony and professional communication equipment.

DESCRIPTION

NPN switching transistor in an SC-70 (SOT323) plastic package. PNP complement: PMSS3906.

MARKING CODE

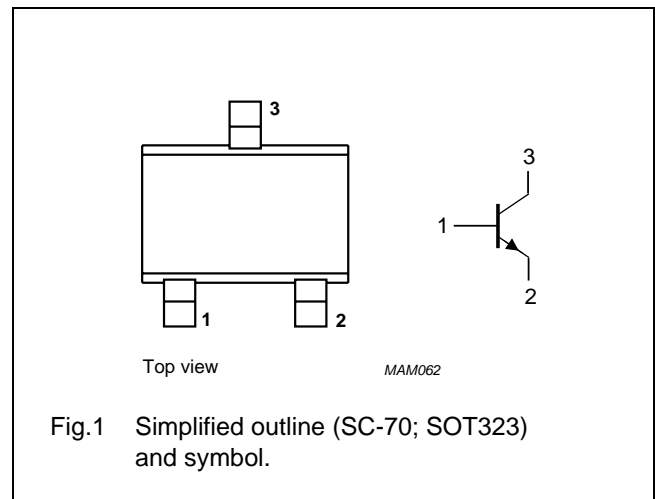
TYPE NUMBER	MARKING CODE ⁽¹⁾
PMSS3904	*04

Note

- * = - : Made in Hong Kong.
* = t : Made in Malaysia.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	-	60	V
V_{CEO}	collector-emitter voltage	open base	-	40	V
V_{EBO}	emitter-base voltage	open collector	-	6	V
I_C	collector current (DC)		-	100	mA
I_{CM}	peak collector current		-	200	mA
I_{BM}	peak base current		-	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	-	200	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	150	°C
T_{amb}	operating ambient temperature		-65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

NPN switching transistor

PMSS3904

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	625	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = 30\text{ V}$	–	50	nA
		$I_E = 0; V_{CB} = 30\text{ V}; T_j = 150\text{ °C}$	–	10	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	50	nA
h_{FE}	DC current gain	$V_{CE} = 1\text{ V}$; see Fig.2			
		$I_C = 0.1\text{ mA}$	40	–	
		$I_C = 1\text{ mA}$	70	–	
		$I_C = 10\text{ mA}$	100	300	
		$I_C = 50\text{ mA}$; note 1	60	–	
		$I_C = 100\text{ mA}$; note 1	30	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 1\text{ mA}$	–	200	mV
		$I_C = 50\text{ mA}; I_B = 5\text{ mA}$; note 1	–	300	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 1\text{ mA}$	650	850	mV
		$I_C = 50\text{ mA}; I_B = 5\text{ mA}$; note 1	–	950	mV
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = 5\text{ V}; f = 1\text{ MHz}$	–	4	pF
C_e	emitter capacitance	$I_C = i_c = 0; V_{EB} = 0.5\text{ V}; f = 1\text{ MHz}$	–	12	pF
f_T	transition frequency	$I_C = 10\text{ mA}; V_{CE} = 20\text{ V}; f = 100\text{ MHz}$	180	–	MHz
F	noise figure	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}; R_S = 1\text{ k}\Omega$ $f = 10\text{ Hz to }15.7\text{ KHz}$	–	5	dB

Switching times (between 10% and 90% levels); see Fig.3

t_{on}	turn-on time	$I_{Con} = 10\text{ mA}; I_{Bon} = 1\text{ mA};$ $I_{Boff} = -1\text{ mA}; V_{CC} = 3\text{ V};$ $V_{BB} = -1.9\text{ V}$	–	110	ns
t_d	delay time		–	50	ns
t_r	rise time		–	60	ns
t_{off}	turn-off time		–	1200	ns
t_s	storage time		–	1000	ns
t_f	fall time		–	200	ns

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

NPN switching transistor

PMSS3904

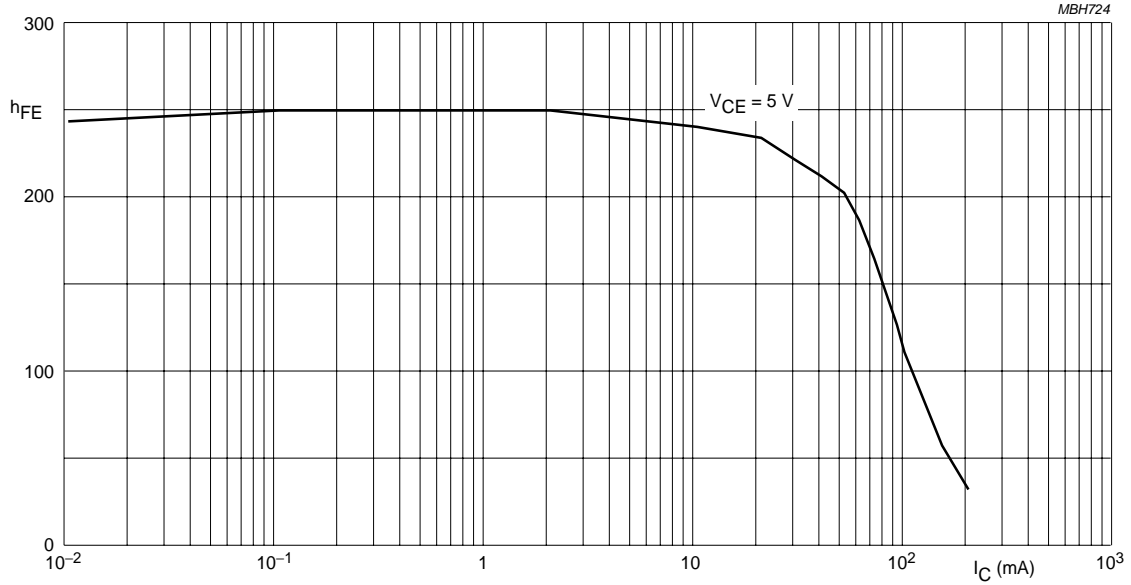
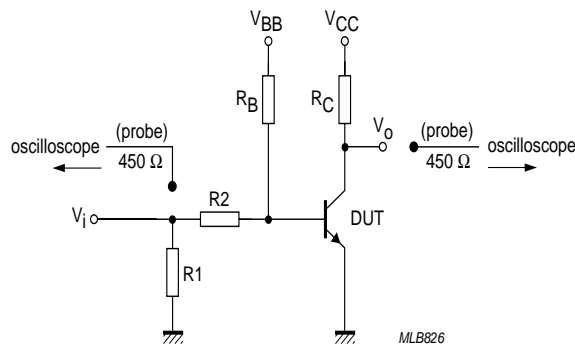


Fig.2 DC gain current; typical values.



$V_i = 5\text{ V}$; $T = 500\ \mu\text{s}$; $t_p = 10\ \mu\text{s}$; $t_r = t_f \leq 3\ \text{ns}$.
 $R_1 = 56\ \Omega$; $R_2 = 2.5\ \text{k}\Omega$; $R_B = 3.9\ \text{k}\Omega$; $R_C = 270\ \Omega$.
 Oscilloscope: input impedance $Z_i = 50\ \Omega$.

Fig.3 Test circuit for switching times.

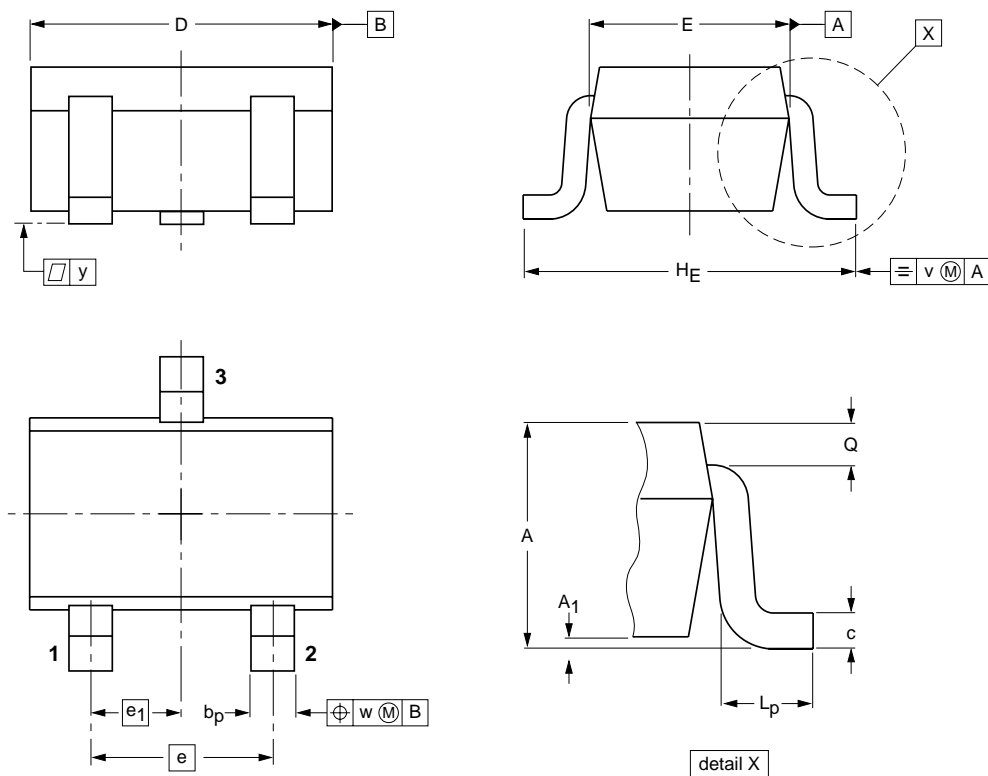
NPN switching transistor

PMSS3904

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

NPN switching transistor

PMSS3904

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

DISCLAIMERS

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions

above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors. No changes were made to the content, except for the legal definitions and disclaimers.

Contact information

For additional information please visit: **<http://www.nxp.com>**

For sales offices addresses send e-mail to: **salesaddresses@nxp.com**

© NXP B.V. 2009

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

115002/04/pp7

Date of release: 1999 May 27

Document order number: 9397 750 05965

