PAM2842

HIGH POWER LED DRIVER

Description

The PAM2842 is a high power LED driver, capable of driving up to 10 high power LEDs in series. The PAM2842 supports buck, boost and sepic topology.

The PAM2842 features over current protection, over voltage protection, under voltage lockout and over temperature protection, which prevent the device from damage.

LED dimming can be done by using a PWM signal to the COMP pin.

The PAM2842 is available in TSSOP-20 packages.

Features

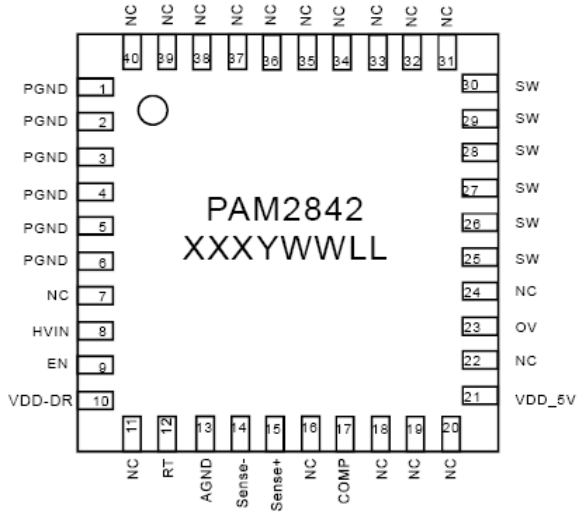
- Output Power up to 30W
- Chip Enable with Soft-start
- Analog and PWM Dimming
- Peak Efficiency up to 97%
- Low Quiescent Current
- Switching Frequency Adjustable
- Support Buck/Boost/Sepic Toplogy
- Over Current Protection
- Over Voltage Protection
- Thermal Protection
- UVLO
- Tiny Pb-Free Packages: 40-Pin QFN6x6 and TSSOP-20

Applications

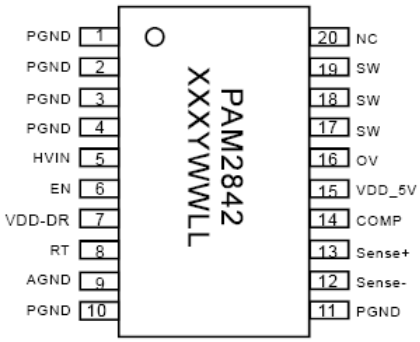
- Home Lighting
- Automotive Lighting
- Monitor Backlighting

Pin Assignments

Top View
6mm*6mm QFN

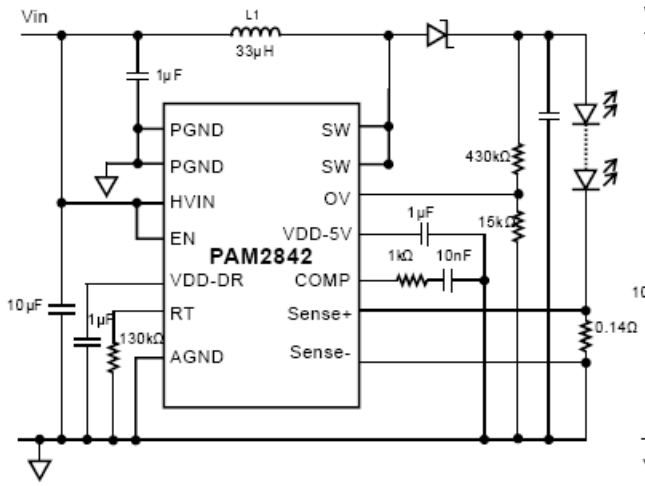


TOP View
TSSOP-20

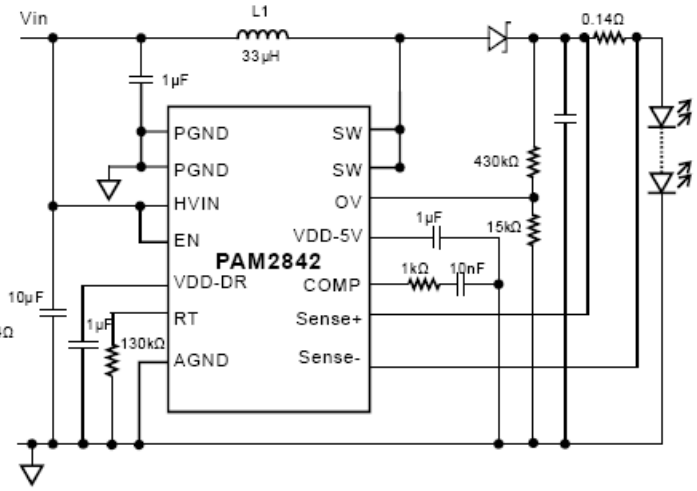


Typical Applications Circuit

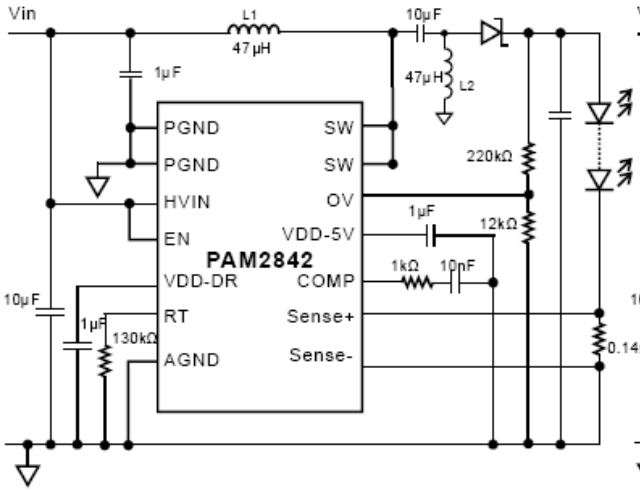
Boost with Low Side Current Sense



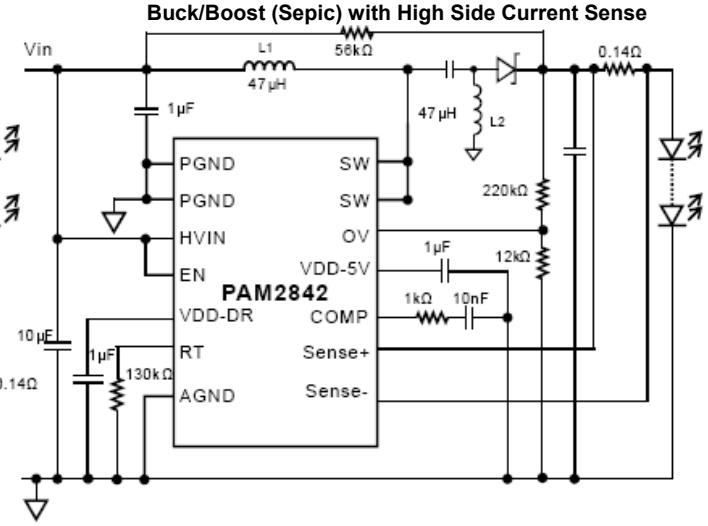
Boost with High Side Current Sense



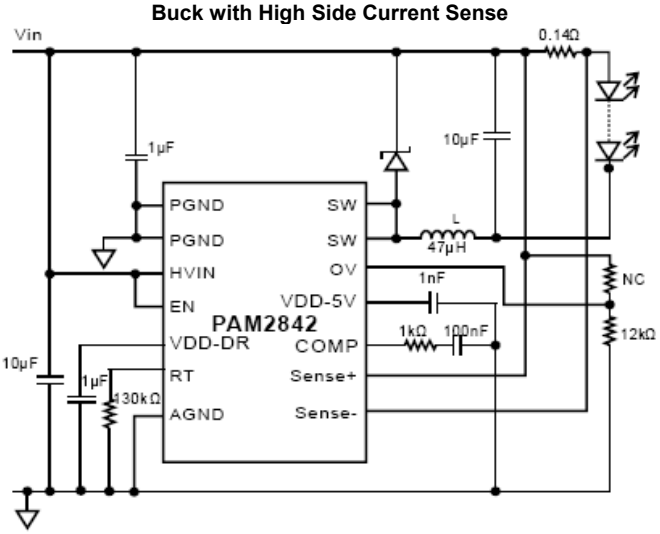
Buck/Boost (Sepic) with Low Side Current Sense



Buck/Boost (Sepic) with High Side Current Sense



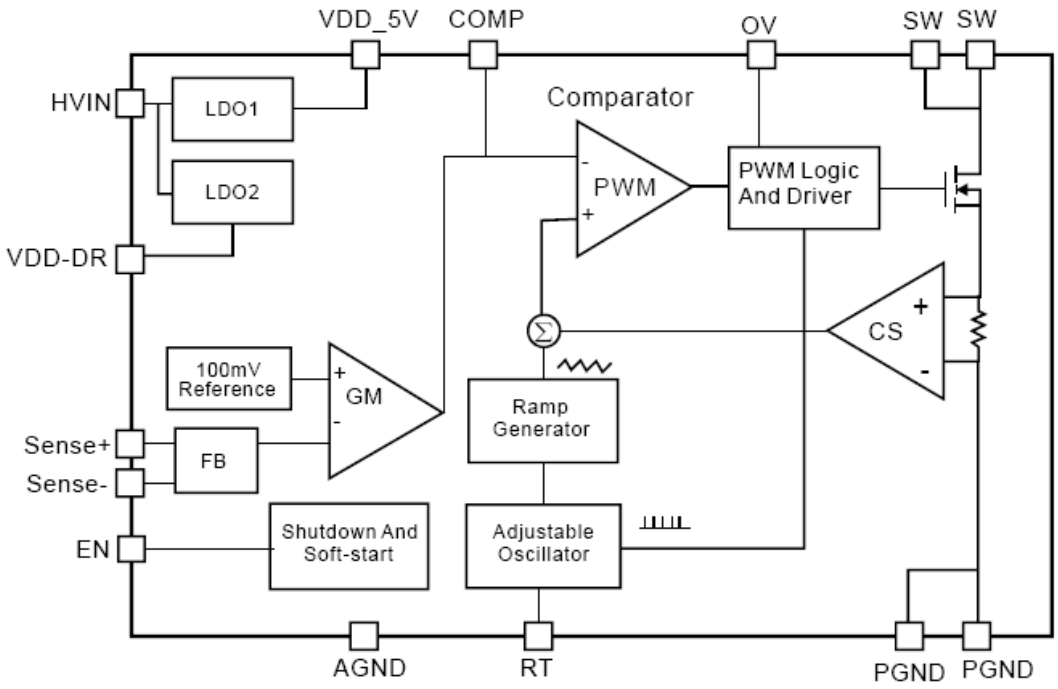
Buck with High Side Current Sense



Pin Descriptions

Pin Name	Pin Number		Function
	QFN6x6-40	TSSOP-20	
PGND	1 – 6	1, 2, 3, 4, 10, 11	Power Ground
HVIN	8	5	Input
EN	9	6	Chip Enable, Active High
VDD-DR	10	7	Internal LDO Output
RT	12	8	Frequency Adjustment Pin
AGND	13	9	Analog Ground
Sense-	14	12	Sense Resistor -
Sense+	15	13	Sense Resistor+
COMP	17	14	Compensation Node
VDD_5V	21	15	Internal LDO Output
OV	23	16	Over Voltage
SW	25 – 30	17, 18, 19	Drain of Main Switch
NC	7, 11, 16, 18-20, 22, 24, 31-40	20	Not Connected

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Supply Voltage	40	V
Buck Application Maximum Output Current	3	A
I/O Pin Voltage Range	GND -0.3 to V_{DD} +0.3	V
Maximum Junction Temperature	150	°C
Storage Temperature	-40 to +150	
Soldering Temperature	300, 5sec	

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage Range	5.5 to 40	V
Operation Temperature Range	-40 to +85	°C
Junction Temperature Range	-40 to +125	

Thermal Information

Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Case)	TSSOP-20	θ_{JC}	20	°C/W
	QFN6x6-40		7.6 (Note 1)	
Thermal Resistance (Junction to Ambient)	TSSOP-20	θ_{JA}	90	
	QFN6x6-40		18.1 (Note 1)	

Note: 1. The exposed PAD must be soldered to a thermal land on the PCB.

Electrical Characteristics (@T_A = +25°C, V_{EN} = V_{DD} = 24V, 1W x 10 LEDs, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Units
Input Voltage Range		5.5		40	V
Quiescent Current	E NA = high (no switching frequency)		1	2	mA
	E NA = high (1M switching frequency)		6		mA
	E NA = high (500k switching frequency)		3		mA
	E NA = high (200k switching frequency)		1.6		mA
	E NA = low		5	10	μA
Feedback Voltage, Low Side	V_{FB} = V_{SENSE+} -AGND, V_{SENSE-} = AGND	95	100	105	mV
Feedback Voltage, High Side	V_{FB} = V_{SENSE+} – V_{SENSE-}	95	100	105	mV
LED Current Line Regulation	I_O = 350mA		0.02		%/V
LED Current Load Regulation			1.0		%
VDD_DR UVLO Hysteresis	No Switching		200		mV

Electrical Characteristics (cont.) (@T_A = +25°C, V_{EN} = V_{DD} = 24V, 1W x 10 LEDs, unless otherwise specified.)

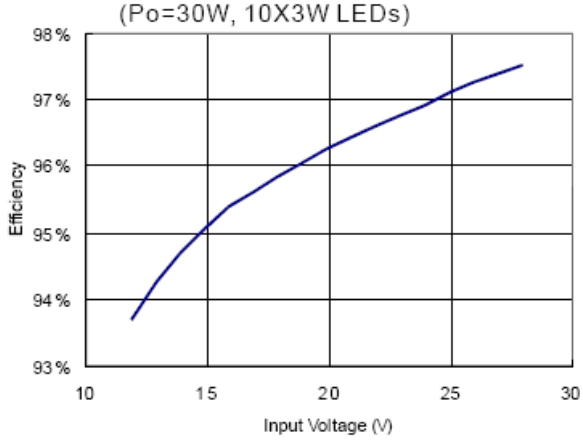
Parameter	Test Conditions	Min	Typ	Max	Units
LDO Stage					
VDD_5V	No Switching	4.5	5	5.5	V
VDD_5V Current Limit	No Switching	14	74	90	mA
VDD_5V UVLO Threshold	No Switching	3.7	4.0	4.3	V
VDD_5V UVLO Hysteresis	No Switching		200		mV
VDD_DR	No Switching	4.5	5	5.5	V
VDD_DR Current_Limit	No Switching	14	50	90	mA
VDD_DR UVLO Threshold	No Switching	3.7	4.0	4.3	V
Switch Stage					
Switch RDS(ON)	VDD_5V = 5V		0.1		Ω
Switch Current Limit			3.5		A
Switch Leakage Current			50		μA
RT Voltage	R_{RT} = 71kΩ	1.1	1.2	1.3	V
Switching Frequency (Note 2)	R_{RT} = 30kΩ	800k	1M	1.2M	Hz
	R_{RT} = 71kΩ	400	500	600	kHz
	R_{RT} = 180kΩ	160	200	240	kHz
Min Duty Cycle	F_{SW} = 1MHz		10		%
	F_{SW} = 500kHz		5		%
	F_{SW} = 200kHz		2.5		%
Max Duty Cycle	Low Side Sense		95		%
	High Side Sense		100		%
VC Source Current	Feedback Voltage = 0		30		μA
VC Sink Current	Feedback Voltage = 0		30		μA
Fault Protection					
OV Threshold Voltage		1.1	1.2	1.3	V
OV Hysteresis			70		mV
Thermal Shutdown			150		°C
Thermal Shutdown Hysteresis			30		°C
Control Interface					
EN High		1.5			V
EN Low				0.4	V

Note: 2. Switching frequency $F_{SW} = \frac{10^{12}}{24x(R_{RT} + 12k)}$, reference value.

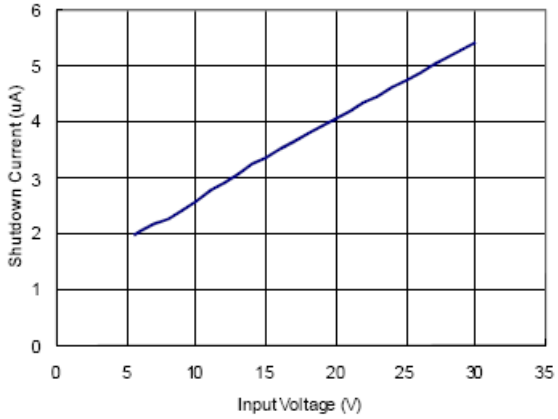
Typical Performance Characteristics

Boost Mode, @T_A = +25°C, V_{EN} = V_{DD} = 24V, 3W LEDs, F_{SW} = 200kHz, unless otherwise specified.)

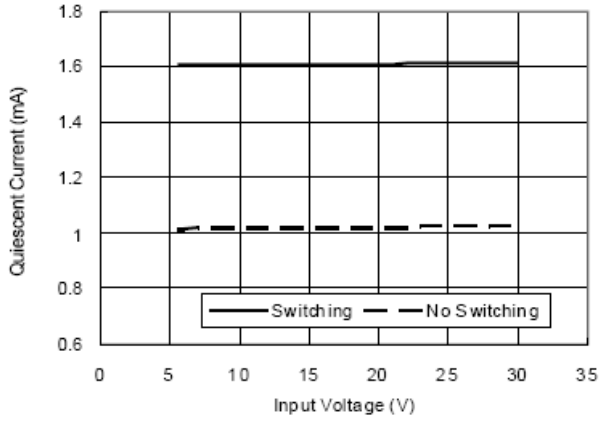
1. Efficiency vs Input Voltage
(Po=30W, 10X3W LEDs)



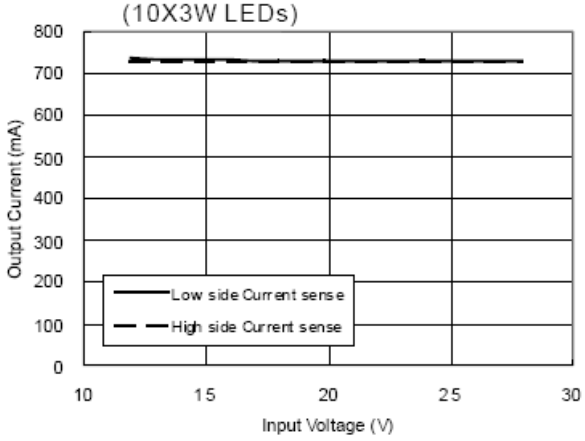
2. Shutdown Current vs Input Voltage



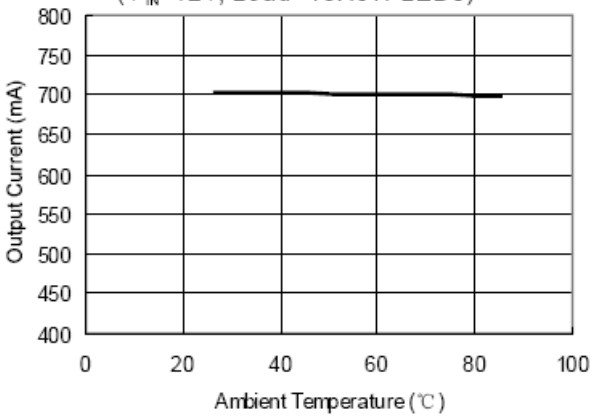
3. Quiescent Current vs Input Voltage



4. Output Current vs Input Voltage
(10X3W LEDs)

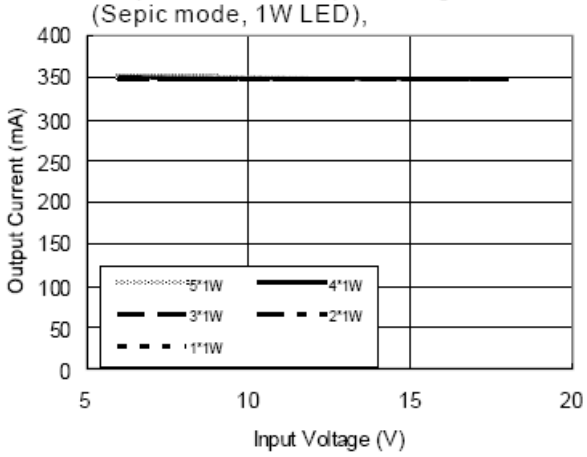


5. Output Current vs Temperature
(V_{IN}=12V, Load=10X3W LEDs)

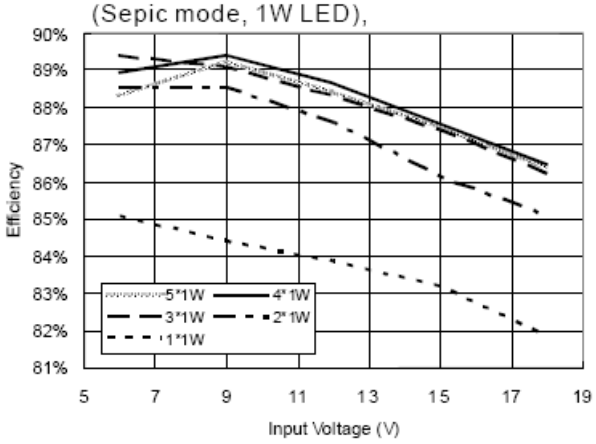


Typical Performance Characteristics (cont.) @T_A = +25°C, F_{SW} = 300kHz, unless otherwise specified.)

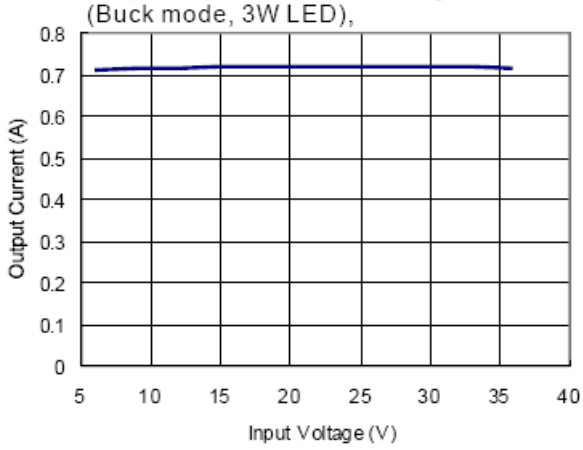
6. Output Current vs Input Voltage
(Sepic mode, 1W LED),



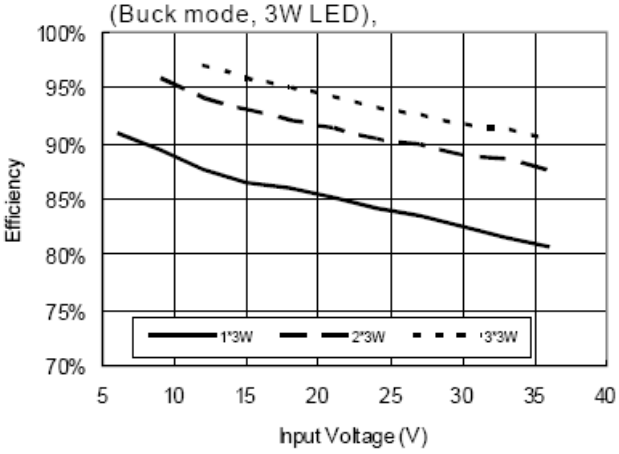
7. Efficiency vs Input Voltage
(Sepic mode, 1W LED),



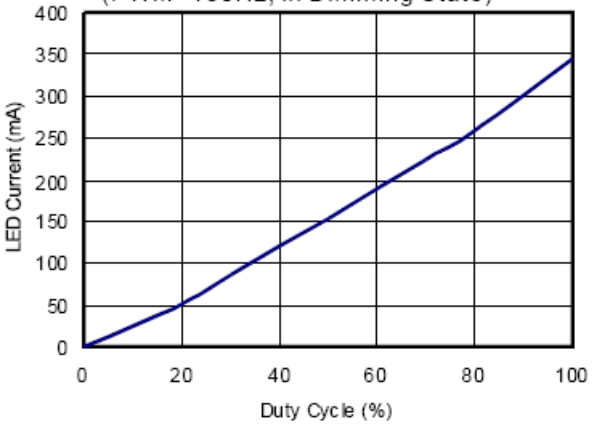
8. Output Current vs Input Voltage
(Buck mode, 3W LED),



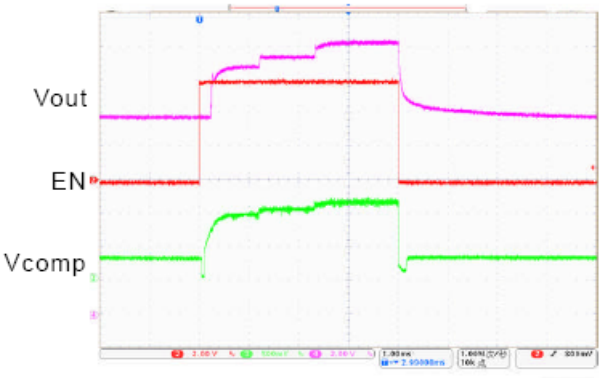
9. Efficiency vs Input Voltage
(Buck mode, 3W LED),



10. LED Current vs Duty Cycle
(PWM=100Hz, in Dimming State)



11. Start up and Shutdown



Application Information

Topology Selection

When maximum power supply voltage is below than minimum load voltage, select the boost topology. When minimum power supply voltage is high than maximum load voltage, select buck topology. When load voltage range is small and between the power supply voltage, select sepic topology.

Table 1: Voltage Condition vs. Topology

Condition	Topology
$V_{INMAX} < V_{OMIN}$	Boost
$V_{INMIN} > V_{OMAX}$	Buck
$V_O < V_{IN}$	Sepic

Inductor Selection

The inductance, peak current rating, series resistance, and physical size should all be considered when selecting an inductor. These factors affect the converter's operating mode, efficiency, maximum output load capability, transient response time, output voltage ripple, and cost.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Large inductance can minimizes the current ripple, and therefore reduces the peak current, which decreases core losses in the inductor and I2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increases physical size and I2R copper losses in the inductor. Low inductor values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves the compromises among circuit efficiency, inductor size, and cost.

When choosing an inductor, the first step is to determine the operating mode: continuous conduction mode (CCM) or discontinuous conduction mode (DCM). When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small-size inductor is required, DCM mode can be chosen. In DCM mode, the inductor value and size can be minimized but the inductor ripple current and peak current are higher than those in CCM.

For the large power application, if chose DCM, the peak current will be very large, it will have great electrical stress on the components, so we chose CCM.

When work in CCM mode, a reasonable ripple current is chosen to

$\Delta I_L = 0.4 I_L$

For the boost topology,

$$I_L = \frac{I_O}{1-D},\ D = \frac{V_O - V_{IN}}{V_O},\ \Delta I_L = \frac{V_{IN}(V_O - V_{IN})}{LF\,V_O}$$

D: duty cycle, Io: output current, F: switching frequency.

From above equation we can get the inductance:

$$L = \frac{2.5 V_{IN}^2 (V_O - V_{IN})}{F I_O V_O^2}$$

The inductor's current rating should be higher

than $I_L + \frac{I_O}{2}$

For the buck topology, $I_L = I_O$

$$D = \frac{V_O}{V_{IN}}$$

$$\Delta I_L = \frac{(V_{IN} - V_O)V_O}{LFV_{IN}\,V_{IN}}$$

so $$L = \frac{2.5 V_O (V_{IN} - V_O)}{F I_O V_O^2}$$

Application Information (cont.)

Inductor Selection (cont.)

For the sepic topology, L1 = L2

$$I_{L1} = I_O \frac{I_O}{1-D}$$

$$I_{L2} = I_O$$

$$D = \frac{V_O}{V_{IN} + V_O}$$

$$\Delta I_L = \frac{V_{IN} V_O}{LF(V_{IN} + V_O)}$$

Chose $\Delta I_L = 0.4 I_{L1}$

so $$L = \frac{2.5 V_{IN}^2}{F I_O (V_{IN} + V_O)}$$

Capacitor Selection

An input capacitor is required to reduce the input ripple and noise for proper operation of the PAM2842. For good input decoupling, Low ESR (equivalent series resistance) capacitors should be used at the input. At least 10μF input capacitor is recommended for most applications. And close the IC V_{IN}-P_{IN} we should add a bypass capacitor, usually use a 1μF capacitor.

A minimum output capacitor value of 10μF is recommended under normal operating conditions, while a 22μF or higher capacitor may be required for higher power LED current. A reasonable value of the output capacitor depends on the LED current. The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging on the output capacitor, and the ohmic ripple due to the capacitor's equivalent series resistance. The ESR of the output capacitor is the important parameter to determine the output voltage ripple of the converter, so low ESR capacitors should be used at the output to reduce the output voltage ripple. The voltage rating and temperature characteristics of the Output capacitor must also be considered. So a value of 10μF, 50V voltage rating capacitor is chosen.

Consider from discharge aspect: I x Δt = C x ΔV

In boost and sepic topology, $C_O = \frac{I_O D}{F V_{RIPPLE}}$

In buck topology, $C_O = \frac{I_O (1-D)}{F V_{RIPPLE}}$

V_{RIPPLE} : Output voltage allowable ripple.

Consider from equivalent series resistance:

$V_{RIPPLE-ESR} = I_{CO.RIPPLE} \times C_{OESR}$

In sepic topology, there is a series capacitor Cs between L1 and L2 (see application schematic), it flows the current:

$$I_{CS(RMS)} = I_O \sqrt{\frac{V_O}{V_{IN}}}$$

The ripple voltage is

$$\Delta V_{CS} = \frac{I_O D}{F C_S}$$

The voltage rating must be higher than input voltage.

Because the Cs capacitor will flow the large RMS current, so this topology is suitable for small power application.

Application Information (cont.)

Diode Selection

PAM2842 is a high switching frequency converter which demands high speed rectifier. It's indispensable to use a Schottky diode rated at 3A, 40V with the PAM2842. Using a Schottky diode with a lower forward voltage drop is better to improve the power LED efficiency.

In boost topology, the voltage rating should be higher than V_{OUT} and in buck topology, the voltage rating higher than V_{IN}, the peak current is

$$I_{D(MAX)} = I_L + \frac{\Delta I_L}{2}$$

in sepic topology, the voltage rating should be higher than V_{IN} +V_{OUT}, the peak current is

$$I_{D(MAX)} = I_{L1(PEAK)} + I_{L2(PEAK)}$$

The average current of the diode equals to I_O.

Work Frequency Selection

PAM2842 working frequency is decided by resistor connect to the RT pin, it can be calculated by follow equation:

$$F_{SW} = \frac{10^{12}}{24x(RT + 12K)}(Hz)$$

From the equations, we can see when working frequency is high, the inductance can be small. It's important in some size limit application. But we should know when the working frequency is higher, the switching loss is higher too. We must pay attention to thermal dissipation in this application.

Methods for Setting LED Current

There are two methods for setting and adjusting the LED current:

1) R_{SENSE} only

2) PWM signal with external components

a) Use the COMP pin

b) Use the Sense pin

- **Method 1: LED Current Setting with Resistor R_{SENSE}**

The most basic means of setting the LED current is connecting a resistor between R_{SENSE}+ and R_{SENSE}-. The LED current is decided by ISET Resistor R_{SENSE}.

$$I_{LED} = 0.1/ R_{SENSE}$$

For flowing the large current, must pay attention to power dissipation on the resistor.

R_{SENSE} has two positions to select: high side current sense and low side current sense. In buck topology it just has high side current sense. In other topology we recommend use low side current sense for easier PCB layout.

- **Method 2: LED Current Setting with PWM Signal Using COMP Pin**

This circuit uses resistor Rsense to set the on state current and the average LED current, then proportional to the percentage of off-time when the COMP pin is logic high. Here use a invert component 2N7002 (Q1) to isolate and invert the PWM signal (See Figure 1).

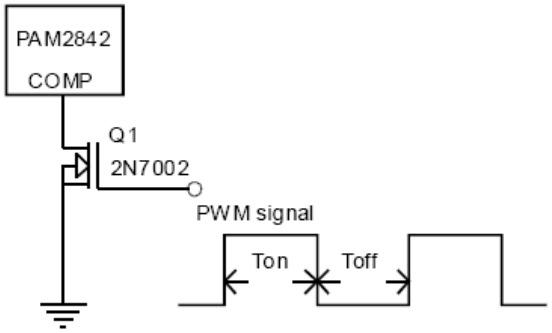


Figure 1. PWM Dimming Use COMP Pin

Average LED current is approximately equal to:

$$I_{AVG} = \frac{T_{OFF} I_{LED}}{T_{ON} + T_{OFF}}$$

Also, the recommended PWM frequency is between 100Hz and 200Hz.

Application Information (cont.)

- **Method 2: LED Current Setting with PWM Signal Using COMP Pin (cont.)**

Frequency <100Hz can cause the LEDs to blink visibly. As the COMP pin connects to a capacitor, it needs rise time. If frequency >200Hz, the average LED current will have a large error when duty cycle is small (<50%).

It maybe generate the audible noise in this dimming condition.

- **Method 3: LED Current Setting with PWM Signal using Sense Pin**

This method is turn PWM signal to DC voltage, the output current can be adjusted. Because the LED current is a adjustable DC value, it will cause LED color drift.

Low side current sense and high side current sense circuit is different. Please see Figure 2 and 3. It use the internal reference voltage, so PWM dimming signal voltage is not considered, just meet the request of the MOSFET driving voltage.

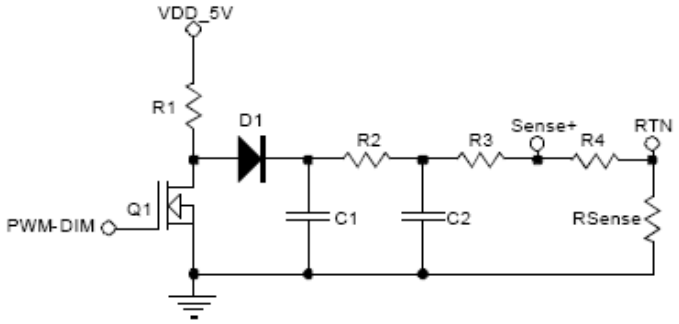


Figure 2. PWM Dimming Use Sense Pin in Low Side Current Sense

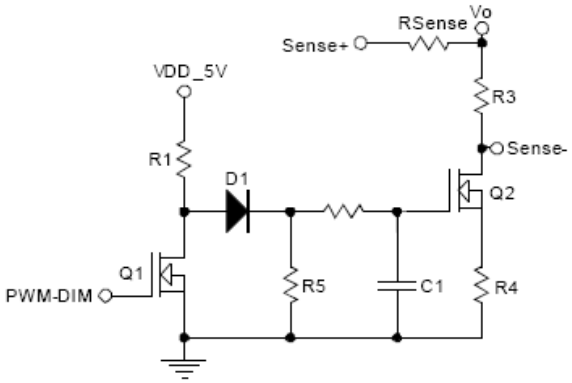


Figure 3. PWM Dimming Use Sense Pin in High Side Current Sense

The RC filter (R1,R2,C1,C2) value is decided by dimming frequency, the divider resistor (R3,R4) is decided by dimming range.

Because final adjusted is a DC value, this method can avoid audible noise effectively and achieve better EMI performance than the second method.

Setting the Output Limit Voltage

The OV pin is connected to the center tap of a resistive voltage divider from the high-voltage output to ground (see application schematic).

$$V_{OUT-LIMIT} = V_{OV}(1+\frac{R_{UP}}{R_{DOWN}})$$

The recommend procedure is to choose R3 = 360K and R4 = 12K to set V_{OUT_LIMIT} = 37.2V.

In boost and sepic circuit, when LED open or no load, the circuit will have no feedback, if no other measure be taken the switch voltage will be very high and damage the switch, so this OV pin must be set carefully.

In buck circuit, the switch voltage is always small than input voltage, so the OV pin setting is not important in this condition.

This OV pin is used to limit output voltage to avoid breakdown of the switch other than to regulate output voltage. The setting value must keep the switch voltage below 40V.

In sepic circuit, one must notice that the switch voltage equals V_{IN} +V_O.

This OV pin has a hysteresis voltage detect function, not latch-up function, so output voltage will have a overshoot when no load or load working voltage is high than setting limit voltage. If the component parameter not match appropriately, the overshoot voltage will be too high and can demage the switch.

Application Information (cont.)

Setting the Output Limit Voltage (cont.)

Several methods can decrease the overshoot voltage:

(1) Add a small capacitor (<100pF) parallel with the up divider resistor (See Figure 4).

(2) Use external zener to clamp the output peak voltage (See Figure 5).

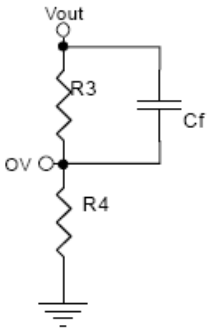


Figure 4. Add Forward Capacitor

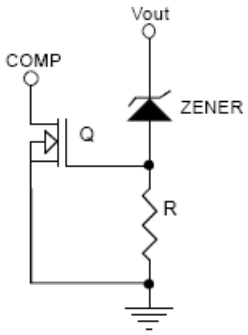


Figure 5. Use External Zener

Note: The output limit voltage must be set higher than working output voltage by a proper value, or it will work abnormal in low temperature or some other conditions.

Short LED Function

PAM2842 is a constant current driver. When one or more LED shorted, the circuit will still work, the output voltage is decided by LED numbers. In boost topology, make sure the output voltage is higher than input voltage; otherwise the unlimited current will directly go through supply to LED and damage the LED.

Power Dissipation

As PAM2842 integrates a power MOSFET, the power dissipation must be considered. To a MOSFET the power loss includes 5 sections, turn on loss, turn off loss, conduction loss, drive loss and output capacitor Coss loss.

$$P_{TURN-ON} = \frac{1}{2} I_{TURN-ON} V_{OUT} T_r f$$

$$P_{TURN-OFF} = \frac{1}{2} I_{TURN-ON} V_{OUT} T_r f$$

$$P_{RDS(ON)} = I_{RMS}^2 R_{DS(ON)}$$

$$P_{DRIVE} = Q_G U_{DRIVE} f$$

$$P_{COSS} = \frac{1}{2} C_{OSS} V_{OUT}^2 f$$

$$P_{SWITCH} = P_{TURN-ON} + P_{TURNE} ff + P_{RDS(ON)} + P_{DRIVE} + P_{COSS}$$

$$\Delta T = \theta_{JA} P_{SWITCH}$$

Tr: switch rise time. Tf: switch fall time. U_{DRIVE}: gate drive voltage. θ_{JA} is relative with IC package, heat-sink area and air flow condition etc.

Above description does not consider the IC control power, so the total power will be more than calculated value.

PAM2842 has over-temperature protection. When junction temperature is over +150°C, it will shut down and auto restart when junction temperature decrease below +120.

In high temperature circumstance application, one must pay attention to heat dissipation, or it will shut down and restart. It is recommended to use external heat-sink and placed near to the IC surface.

Application Information (cont.)

PCB Layout Guidelines

Careful PCB layout is important for normal operation. Use the following guidelines for good PCB layout: (BOOST)

1) Minimize the area of the high current switching loop of the rectifier diode and output capacitor to avoid excessive switching noise.

2) Connect high-cur rent input and output components with short and wide connections. The high-current input loop goes from the positive terminal of the input capacitor to the inductor and the SW pin. The high-current output loop is from the positive terminal of the input capacitor through the inductor, rectifier diode, and positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Avoid using vias in the highcurrent paths. If vias are unavoidable, use multiple vias in parallel to reduce resistance and inductance.

3) Create a ground island (PGND) consisting of the input and output capacitor ground and PGND pin. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground island (AGND) consisting of the output voltage detection-divider ground connection, the Sense-pin connection, V_{CC}-5V and V_{CC}-driver capacitor connections. Connect the device's exposed backside pad to PGND. Make sure no other connections between these separate ground planes.

4) Place the output voltage setting-divider resistors as close to the OV pin as possible. The divider's center trace should be kept short. Avoid running the sensing traces near SW Pin.

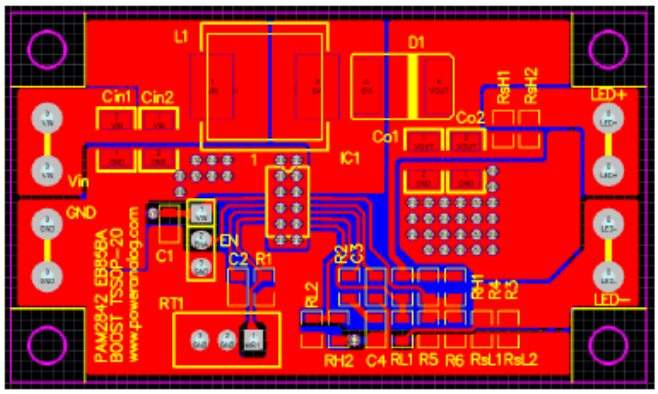
5) Place the VIN pin bypass capacitor as close to the device as possible. The ground connection of the VIN bypass capacitor should be connected directly to GND pins with a wide trace.

6) Minimize the size of the SW node while keeping it wide and short. Keep the SW node away from the feedback node. If possible, avoid running the SW node from one side of the PCB to the other.

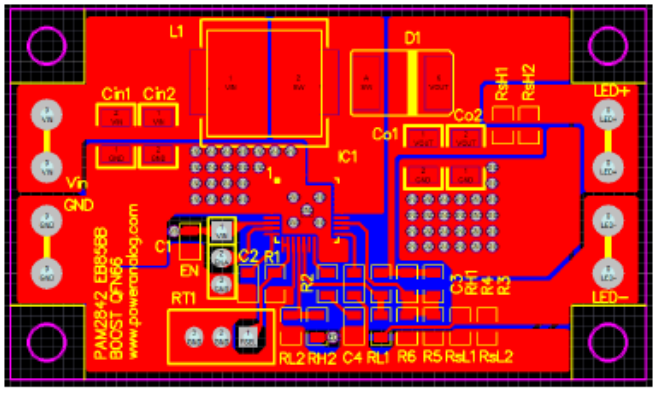
7) For the good thermal dissipation, PAM2842 has a heat dissipate pad in the bottom side, it should be soldered to PCB surface. As the copper area cannot be large in the component side, we can use multiple vias connecting to other side of the PCB.

8) Refer to the example of a PAM2842 Evaluation board layout below.

TSSOP-20 Boost

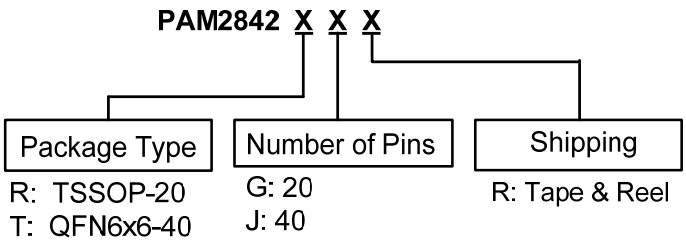


QFN6x6-40 Boost



PCB Layout Example

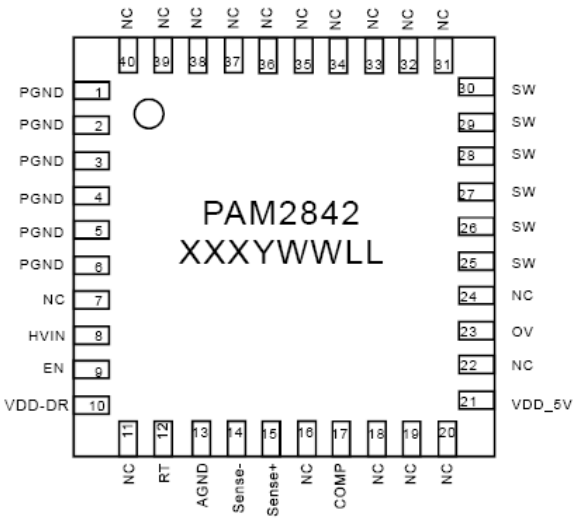
Ordering Information



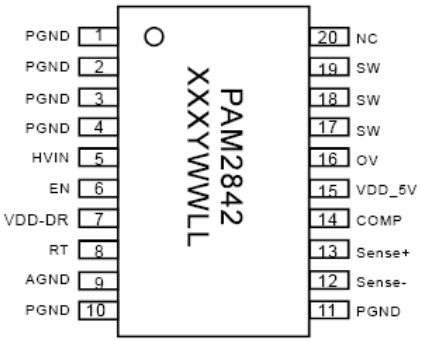
Part Number	Package Type	Standard Package
PAM2842RGR	TSSOP-20	1000 Units/Tape&Reel
PAM2842TJR	QFN6x6-40	1000 Units/Tape&Reel

Marking Information

Top View
6mm*6mm QFN



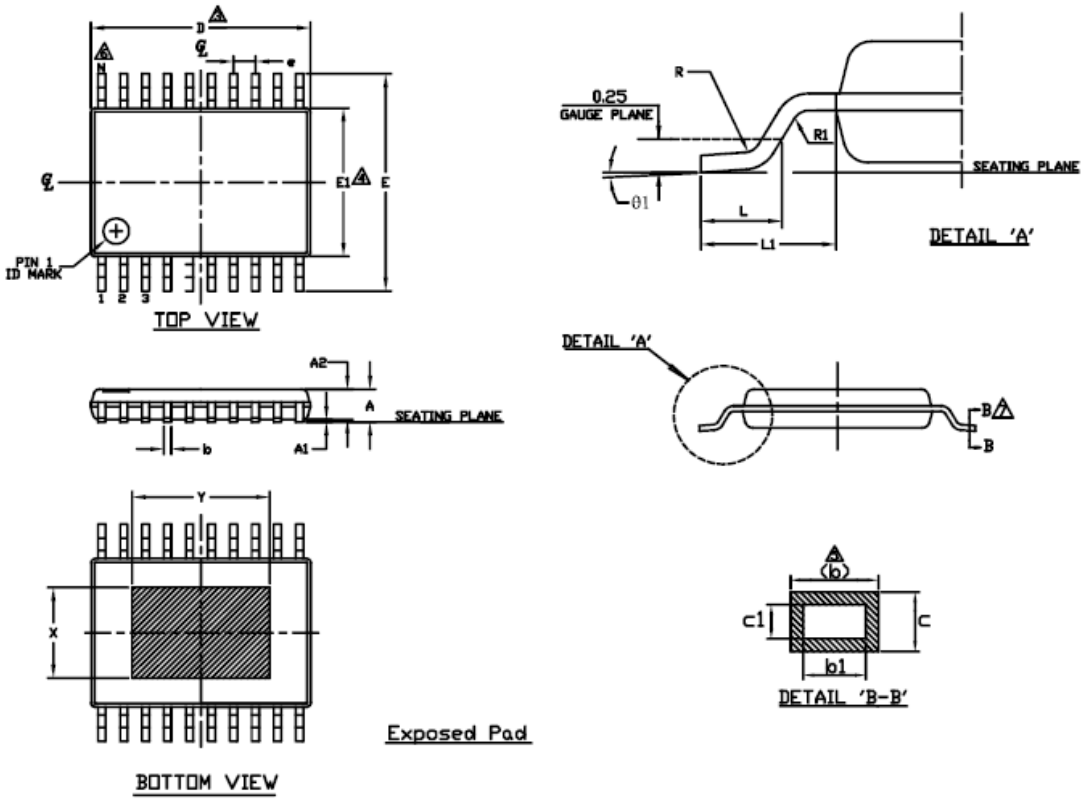
TOP View
TSSOP-20



X: Internal Code
Y: Year
WW: Week
LL: Internal Code

Package Outline Dimensions (All dimensions in mm.)

TSSOP-20



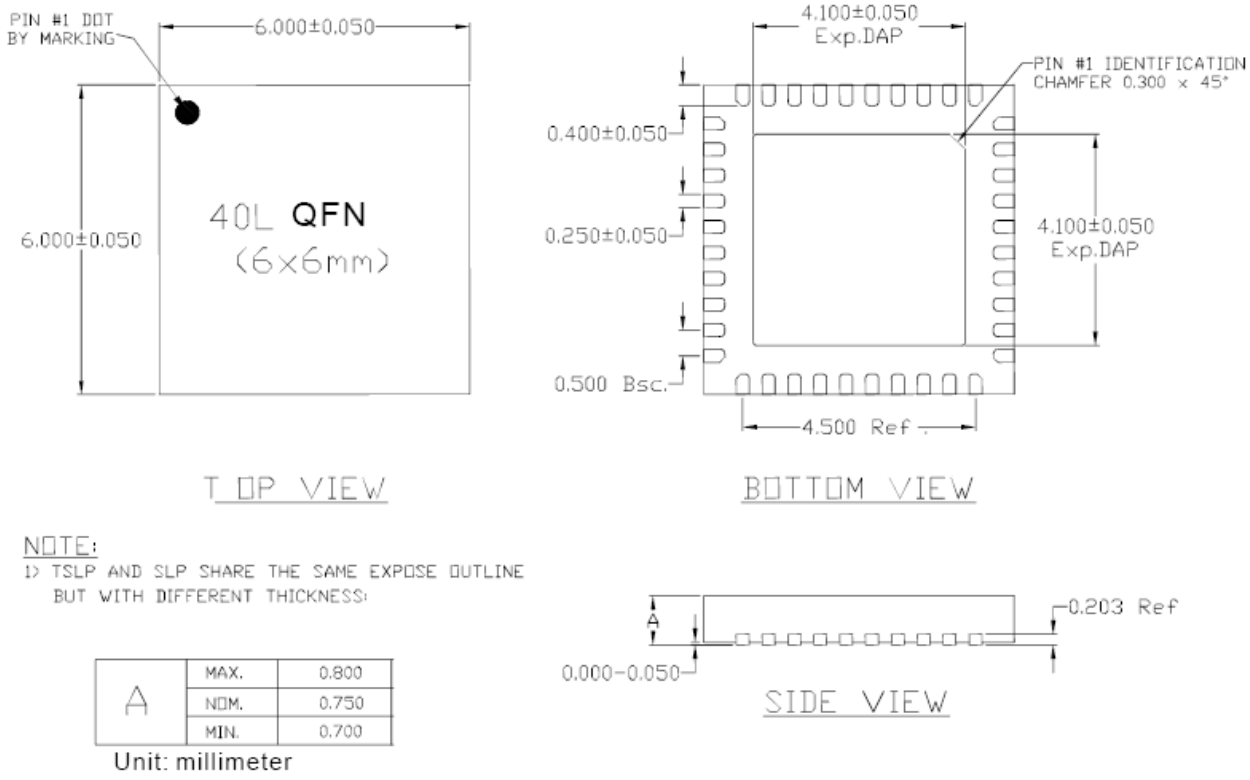
SYMBOL	MIN.	NOM.	MAX.	SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.20	b	0.19	-	0.30
A1	0.025	-	0.100	b1	0.19	0.22	0.25
A2	0.80	0.90	1.05	c	0.09	-	0.20
D	6.4	6.5	6.6	c1	0.09	-	0.16
E1	4.3	4.4	4.5	θ	0°	-	8°
E	6.2	6.4	6.6	L1	1.0 REF		
L	0.45	0.60	0.75	e	0.65 BSC		
R	0.09	-	-	N	20		
R1	0.09	-	-				

Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH ,PROTRUSIONS OR GATE BURRS.
4. DIMENSION 'E1' DOES NOT INCLUDE INTERNAL FLASH OR PROTUSION.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION.
6. 'N' IS THE MAXIMUM NUMBER OF LEAD TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. CROSS SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.
8. EXPOSED PAD WILL BE DEPEND ON THE PAD SIZE OF THE L/F

Package Outline Dimensions (cont.) (All dimensions in mm.)

QFN6x6-40



A	MAX.	0.800
	NOM.	0.750
	MIN.	0.700

Unit: millimeter

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