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# FQD30N06

## N-Channel QFET® MOSFET

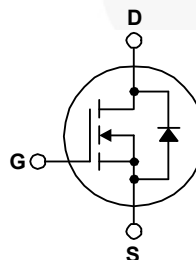
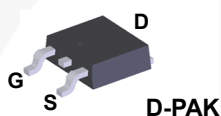
60 V, 22.7 A, 45 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 22.7 A, 60 V,  $R_{DS(on)} = 45 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10\text{V}$ ,  $I_D = 11.4 \text{ A}$
- Low Gate Charge (Typ. 19 nC)
- Low Crss (Typ. 40 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQD30N06TM	Unit
$V_{DSS}$	Drain-Source Voltage	60	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	22.7
		- Continuous ( $T_C = 100^\circ\text{C}$ )	14.3
$I_{DM}$	Drain Current - Pulsed (Note 1)	90.8	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	280	mJ
$I_{AR}$	Avalanche Current (Note 1)	22.7	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	44	W
	- Derate above $25^\circ\text{C}$	0.35	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQD30N06TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.85	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD30N06TM	FQD30N06	D-PAK	Tape and Reel	330 mm	16 mm	2500 units

## Electrical Characteristics T<sub>c</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.06	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 48 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 25 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -25 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11.4 A	--	0.036	0.045	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 11.4 A	--	15	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	725	945	pF
C <sub>oss</sub>	Output Capacitance		--	270	350	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	40	52	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 25 Ω  (Note 4)	--	10	30	ns
t <sub>r</sub>	Turn-On Rise Time		--	85	180	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	35	80	ns
t <sub>f</sub>	Turn-Off Fall Time		--	40	90	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 48 V, I <sub>D</sub> = 30 A, V <sub>GS</sub> = 10 V  (Note 4)	--	19	25	nC
Q <sub>gs</sub>	Gate-Source Charge		--	5.4	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	8.5	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	22.7	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	90.8	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 22.7 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>F</sub> = 30 A	--	45	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs	--	65	--	nC

### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 630 μH, I<sub>AS</sub> = 22.7 A, V<sub>DD</sub> = 25 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 30 A, di/dt ≤ 300 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

## Typical Characteristics

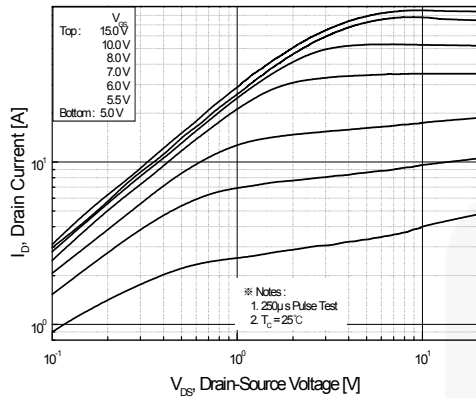


Figure 1. On-Region Characteristics

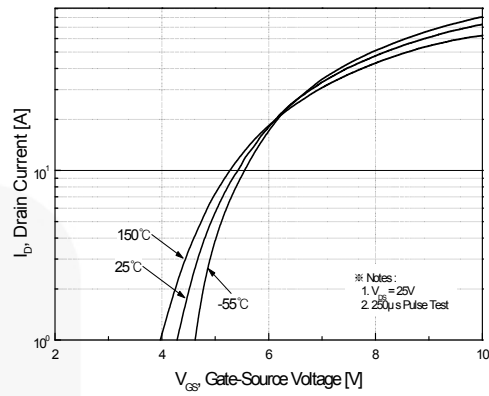


Figure 2. Transfer Characteristics

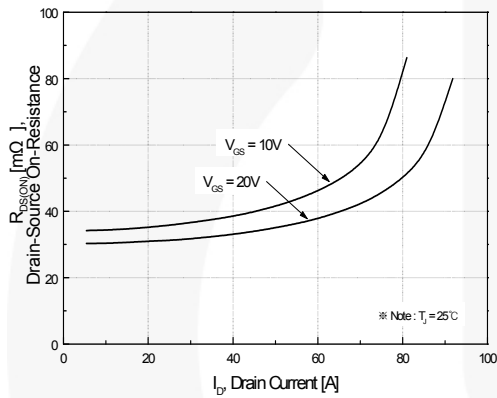


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

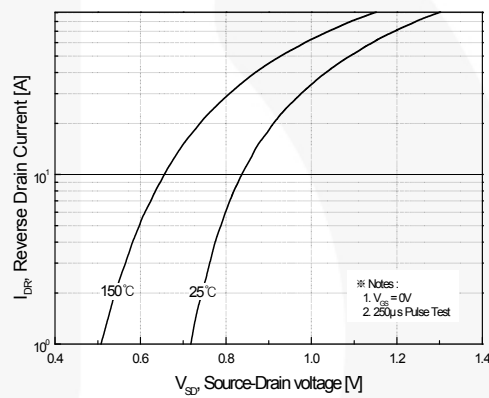


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

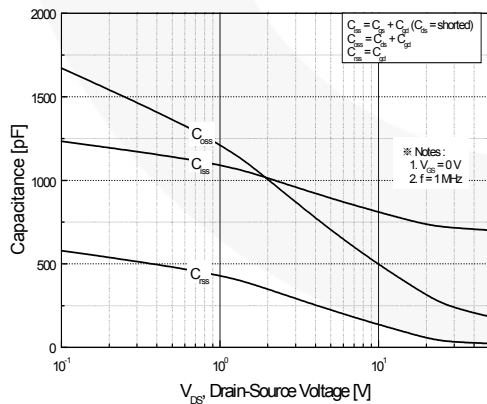


Figure 5. Capacitance Characteristics

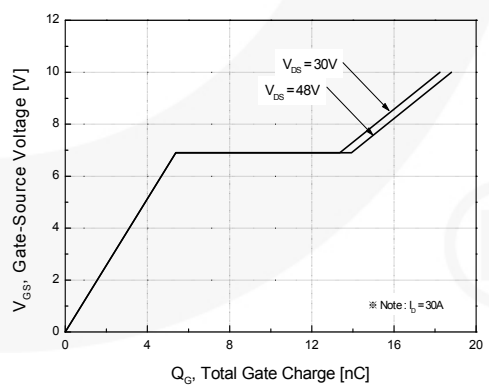
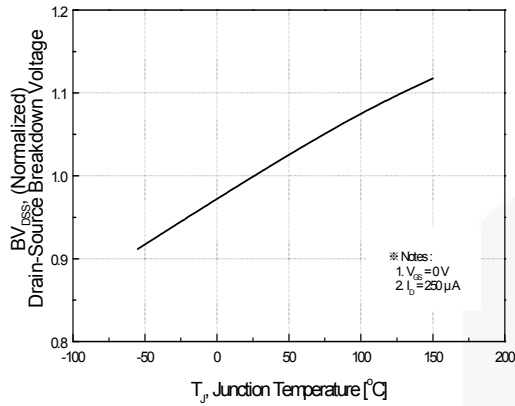
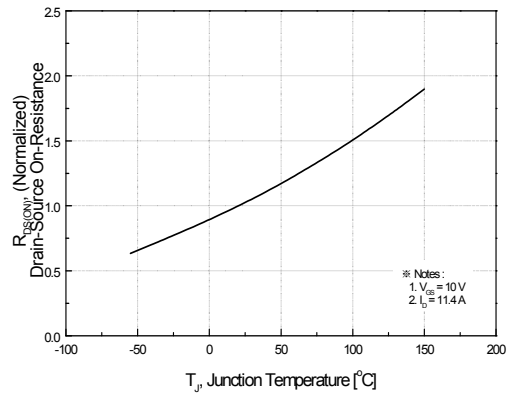


Figure 6. Gate Charge Characteristics

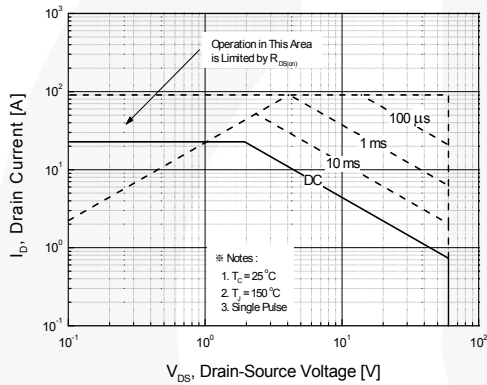
**Typical Characteristics** (Continued)



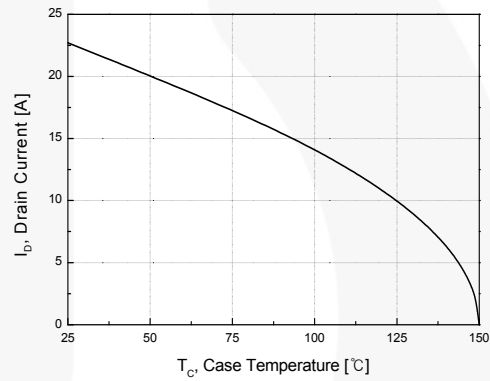
**Figure 7. Breakdown Voltage Variation vs. Temperature**



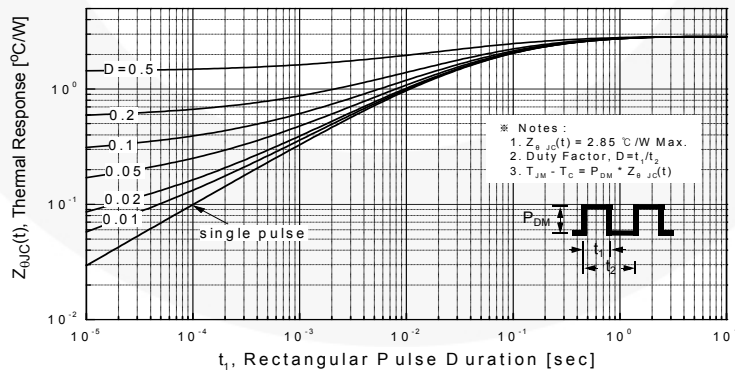
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

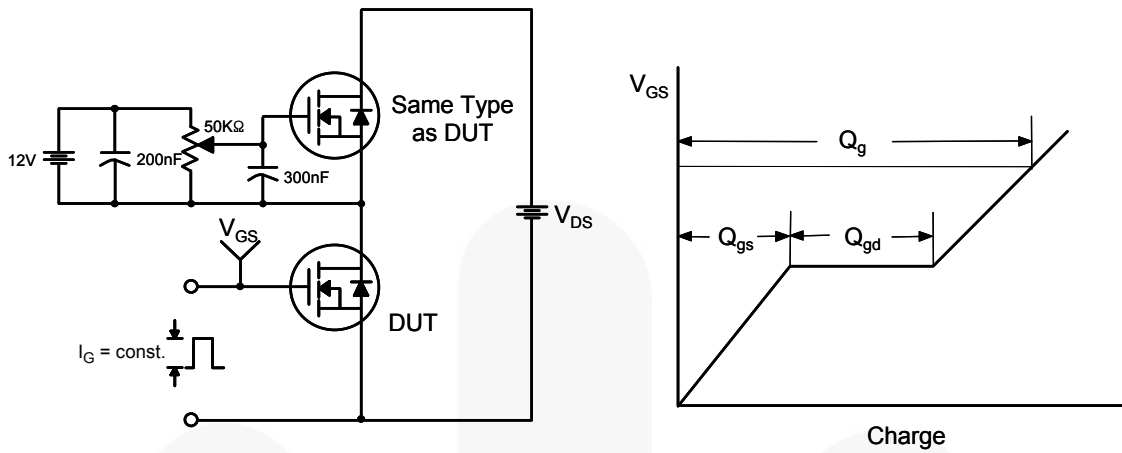


Figure 12. Gate Charge Test Circuit & Waveform

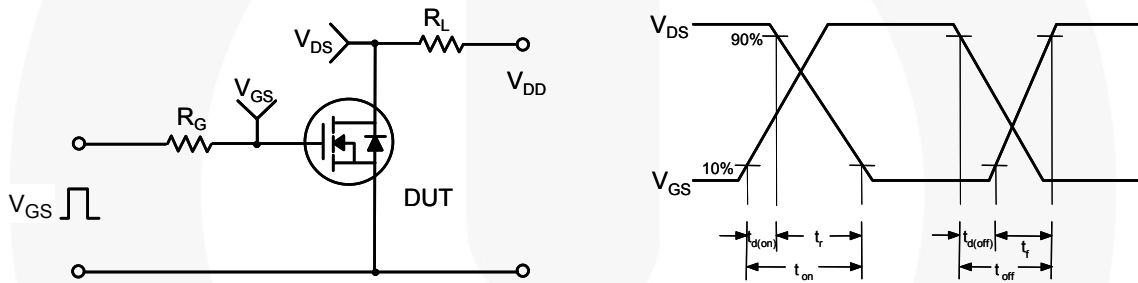


Figure 13. Resistive Switching Test Circuit & Waveforms

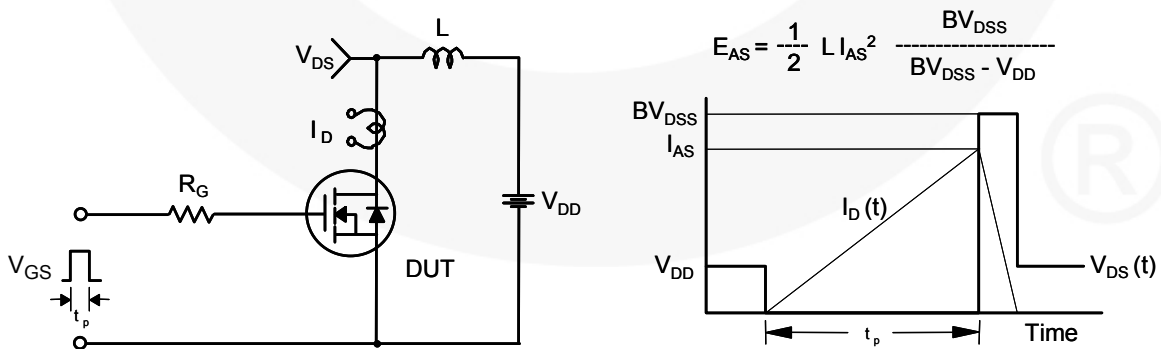


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

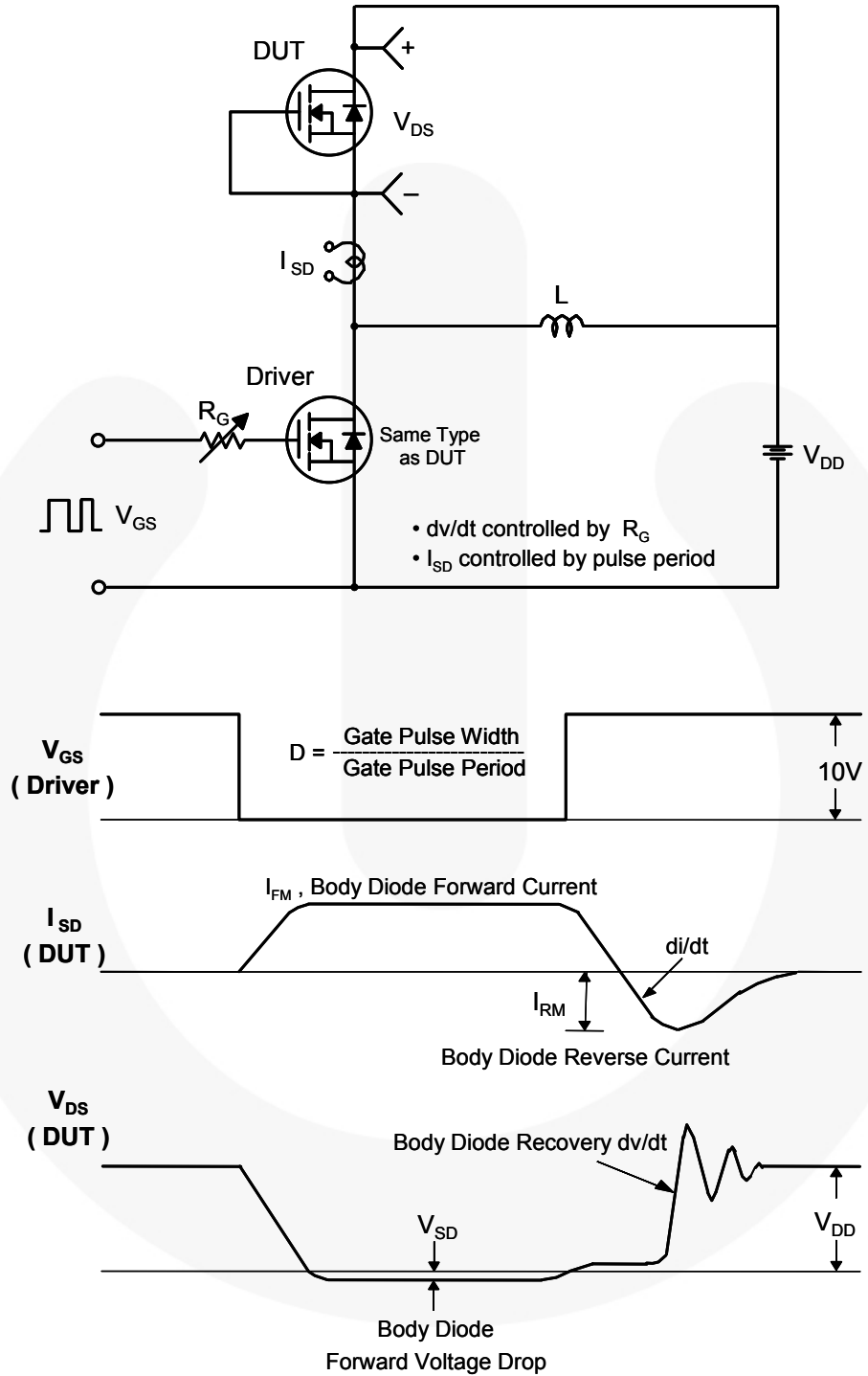
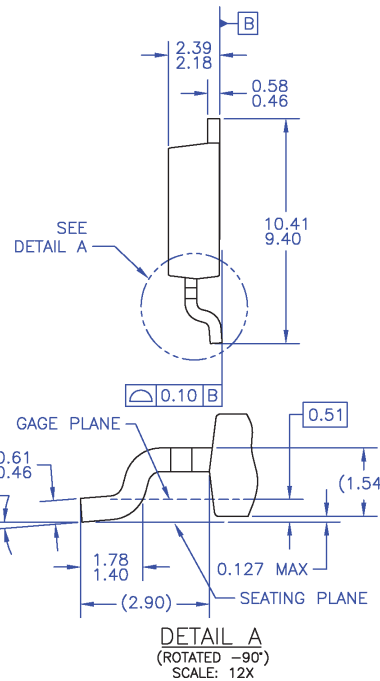
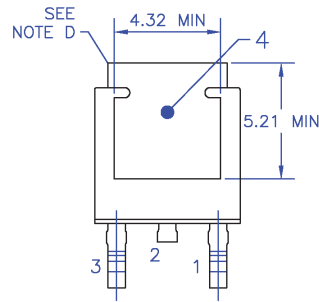
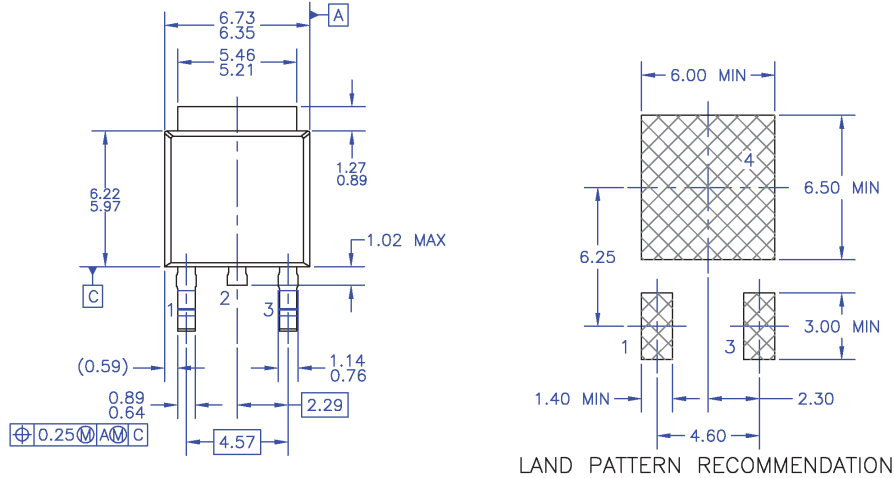


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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