

NuMicro™ NUC200/220 Series Product Brief

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NUMICRO™ NUC200/220 PRODUCT BRIEF

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1 GENERAL DESCRIPTION

The NuMicro™ NUC200 Series 32-bit microcontrollers is embedded with the newest ARM® Cortex™-M0 core with a cost equivalent to traditional 8-bit MCU for industrial control and applications requiring rich communication interfaces. The NuMicro™ NUC200 Series includes NUC200 and NUC220 product lines.

The NuMicro™ NUC200 Advanced Line is embedded with the Cortex™-M0 core running up to 50 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 4 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I²C, I²S, PWM Timer, GPIO, PS/2, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

The NuMicro™ NUC220 USB Line with USB 2.0 full-speed function is embedded with the Cortex™-M0 core running up to 50 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 4 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I²C, I²S, PWM Timer, GPIO, PS/2, USB 2.0 FS Device, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I ² C	USB	LIN	CAN	PS/2	I ² S	SC
NUC200	•	•	•				•	•	•
NUC220	•	•	•	•			•	•	•

Table 1-1 Connectivity Support Table

2 FEATURES

- ARM® Cortex™-M0 core
 - Runs up to 50 MHz
 - One 24-bit system timer
 - Supports low power sleep mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
 - 32K/64K/128K bytes Flash for program code
 - 4 KB flash for ISP loader
 - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
 - 512 byte page erase for flash
 - Configurable data flash address and size for 128 KB system, fixed 4 KB data flash for the 32 KB and 64 KB system
 - Supports 2-wired ICP update through SWD/ICE interface
 - Supports fast parallel programming mode by external programmer
- SRAM Memory
 - 8K/16K bytes embedded SRAM
 - Supports PDMA mode
- PDMA (Peripheral DMA)
 - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
 - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
 - Flexible selection for different applications
 - Built-in 22.1184 MHz high speed oscillator for system operation
 - ◆ Trimmed to $\pm 1\%$ at $+25\text{ }^\circ\text{C}$ and $V_{DD} = 5\text{ V}$
 - ◆ Trimmed to $\pm 3\%$ at $-40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ and $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
 - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
 - Supports one PLL, up to 50 MHz, for high performance system operation
 - External 4~24 MHz high speed crystal input for precise timing operation
 - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
 - Four I/O modes:
 - ◆ Quasi-bidirectional
 - ◆ Push-pull output
 - ◆ Open-drain output
 - ◆ Input only with high impedance
 - TTL/Schmitt trigger input selectable



- I/O pin configured as interrupt source with edge/level setting
- Timer
 - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
 - Independent clock source for each timer
 - Provides one-shot, periodic, toggle and continuous counting operation modes
 - Supports event counting function
 - Supports input capture function
- Watchdog Timer
 - Multiple clock sources
 - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
 - Wake-up from Power-down or Idle mode
 - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
 - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
 - Supports software compensation by setting frequency compensate register (FCR)
 - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - Supports Alarm registers (second, minute, hour, day, month, year)
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - Supports battery power pin (V_{BAT})
 - Supports wake-up function
- PWM/Capture
 - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
 - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
 - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
 - Supports Capture interrupt
- UART
 - Up to three UART controllers
 - UART ports with flow control (TXD, RXD, nCTS and nRTS)
 - UART0 with 64-byte FIFO is for high speed
 - UART1/2(optional) with 16-byte FIFO for standard device
 - Supports IrDA (SIR) and LIN function
 - Supports RS-485 9-bit mode and direction control
 - Programmable baud-rate generator up to 1/16 system clock
 - Supports PDMA mode
- USB 2.0 Full-Speed Device (NUC220 series only)
 - One set of USB 2.0 FS Device 12 Mbps
 - On-chip USB Transceiver



- Provides 1 interrupt source with 4 interrupt events
- Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
- Auto suspend function when no bus signaling for 3 ms
- Provides 6 programmable endpoints
- Includes 512 Bytes internal SRAM as USB buffer
- Provides remote wake-up capability
- SPI
 - Up to four sets of SPI controllers
 - The maximum SPI clock rate of Master can up to 36 MHz (chip working at 5V)
 - The maximum SPI clock rate of Slave can up to 18 MHz (chip working at 5V)
 - Supports SPI Master/Slave mode
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 8 to 32 bits
 - MSB or LSB first data transfer
 - Rx and Tx on both rising or falling edge of serial clock independently
 - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
 - Supports Byte Suspend mode in 32-bit transmission
 - Supports PDMA mode
 - Supports three wire, no slave select signal, bi-direction interface
- I²C
 - Up to two sets of I²C device
 - Master/Slave mode
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - Programmable clocks allowing for versatile rate control
 - Supports multiple address recognition (four slave address with mask option)
 - Supports wake-up function
- I²S
 - Interface with external audio CODEC
 - Operate as either Master or Slave mode
 - Capable of handling 8-, 16-, 24- and 32-bit word sizes
 - Supports mono and stereo audio data
 - Supports I²S and MSB justified data format
 - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
 - Generates interrupt requests when buffer levels cross a programmable boundary
 - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
 - Host communication inhibit and request to send detection
 - Reception frame error detection
 - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
 - Double buffer for data reception
 - Software override bus



- ADC
 - 12-bit SAR ADC with 760 kSPS
 - Up to 8-ch single-end input or 4-ch differential input
 - Single scan/single cycle scan/continuous scan
 - Each channel with individual result register
 - Scan on enabled channels
 - Threshold voltage detection
 - Conversion started by software programming or external input
 - Supports PDMA mode
- Analog Comparator
 - Up to two analog comparators
 - External input or internal Band-gap voltage selectable at negative node
 - Interrupt when compare result change
 - Supports Power-down wake-up
- Smart Card Host (SC)
 - Compliant to ISO-7816-3 T=0, T=1
 - Supports up to three ISO-7816-3 ports
 - Separate receive / transmit 4 bytes entry FIFO for data payloads
 - Programmable transmission clock frequency
 - Programmable receiver buffer trigger level
 - Programmable guard time selection (11 ETU ~ 266 ETU)
 - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
 - Supports auto inverse convention function
 - Supports transmitter and receiver error retry and error limit function
 - Supports hardware activation sequence process
 - Supports hardware warm reset sequence process
 - Supports hardware deactivation sequence process
 - Supports hardware auto deactivation sequence when detecting the card removal
- 96-bit unique ID (UID)
- One built-in temperature sensor with 1°C resolution
- Brown-out Detector
 - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
 - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage level: 2.0 V
- Operating Temperature: -40°C ~ 85°C
- Packages:
 - All Green package (RoHS)
 - LQFP 100-pin / 64-pin / 48-pin



3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC200/220xxxAN Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-bit)	Connectivity						ISO-7816-3	I ² S	PWM (16-bit)	ADC (12-bit)	Comparator	RTC	ISP/ICP/IAP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC200 Advanced Line																				
NUC200LC2AN	32 KB	8 KB	4 KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	2	1	6	7	1	√	√	LQFP48
NUC200LD2AN	64 KB	8 KB	4KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	2	1	6	7	1	√	√	LQFP48
NUC200LE3AN	128 KB	16 KB	Definable	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	2	1	6	7	1	√	√	LQFP48
NUC200SC2AN	32 KB	8 KB	4KB	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	2	1	6	7	2	√	√	LQFP64
NUC200SD2AN	64 KB	8 KB	4KB	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	2	1	6	7	2	√	√	LQFP64
NUC200SE3AN	128 KB	16 KB	Definable	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	2	1	6	7	2	√	√	LQFP64
NUC200VE3AN	128 KB	16 KB	Definable	4 KB	up to 83	4x32-bit	3	4	2	-	-	-	3	1	8	8	2	√	√	LQFP100
NUC220 USB Line																				
NUC220LC2AN	32 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	2	1	4	7	1	√	√	LQFP48
NUC220LD2AN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	2	1	4	7	1	√	√	LQFP48
NUC220LE3AN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	2	1	4	7	1	√	√	LQFP48
NUC220SC2AN	32 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	2	1	6	7	2	√	√	LQFP64
NUC220SD2AN	64 KB	8 KB	8 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	2	1	6	7	2	√	√	LQFP64
NUC220SE3AN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	2	1	6	7	2	√	√	LQFP64
NUC220VE3AN	128 KB	16 KB	Definable	4 KB	up to 79	4x32-bit	3	4	2	1	-	-	3	1	8	8	2	√	√	LQFP100

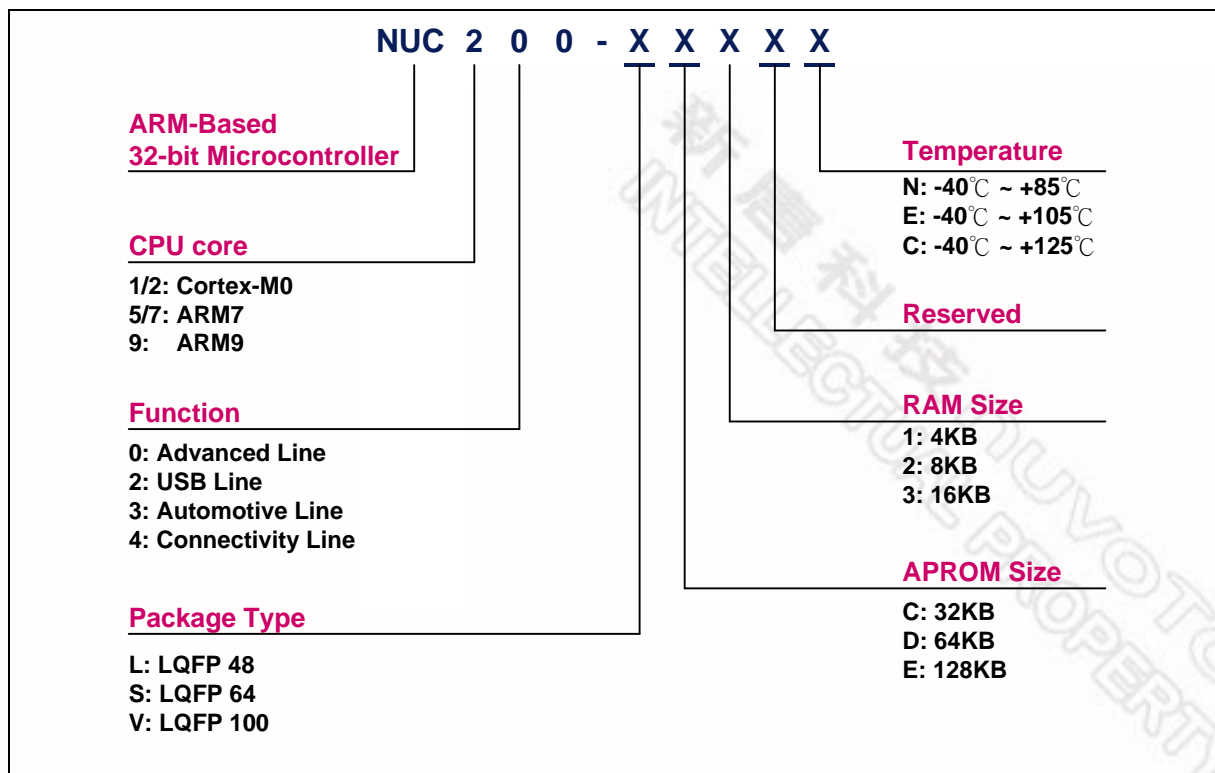


Figure 3-1 NuMicro™ NUC200 Series Selection Code



3.2 Pin Configuration

3.2.1 NuMicro™ NUC200 Pin Diagram

3.2.1.1 NuMicro™ NUC200VxxAN LQFP 100-pin

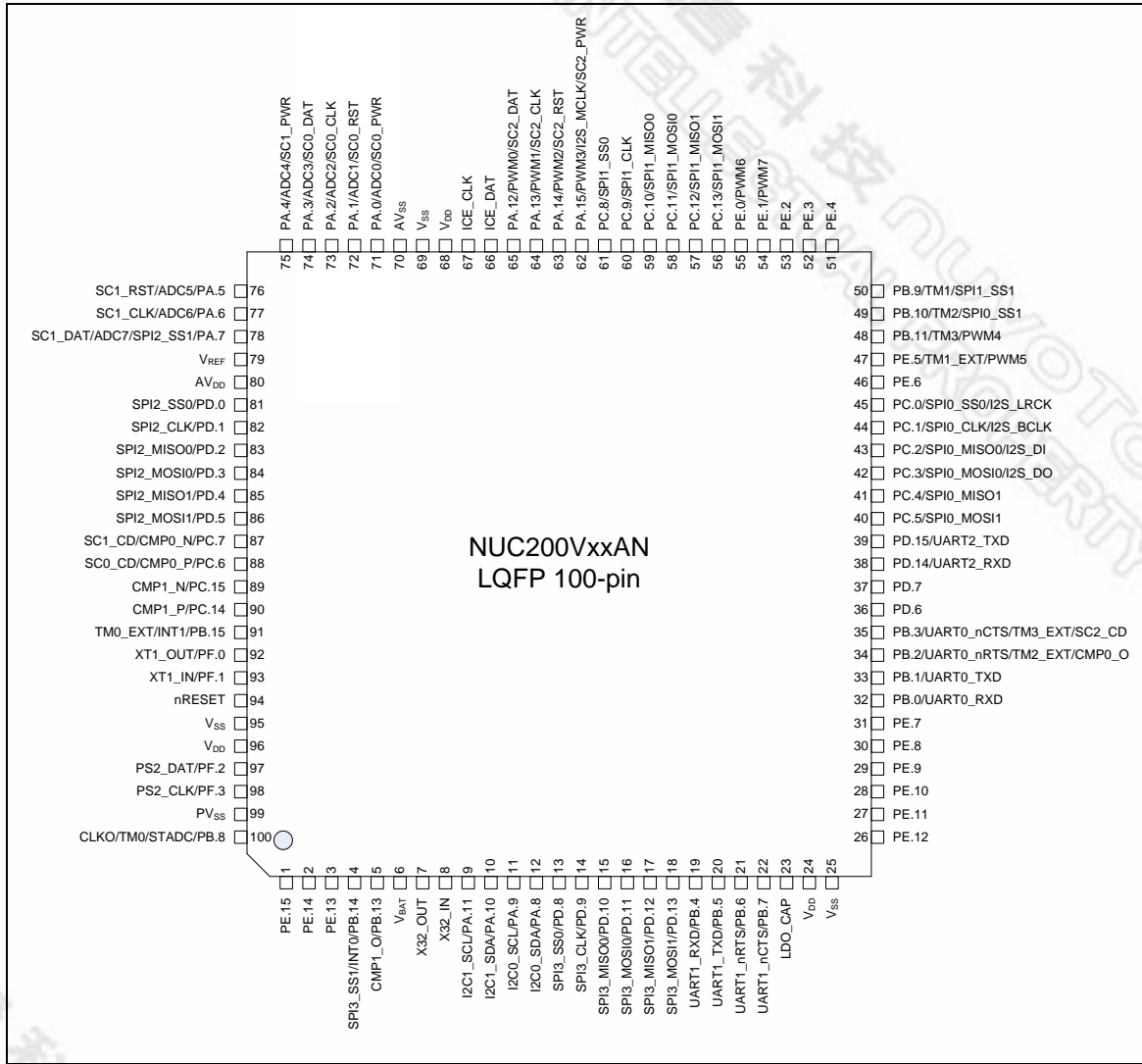


Figure 3-2 NuMicro™ NUC200VxxAN LQFP 100-pin Diagram

3.2.1.2 NuMicro™ NUC200RxxAN LQFP 64-pin

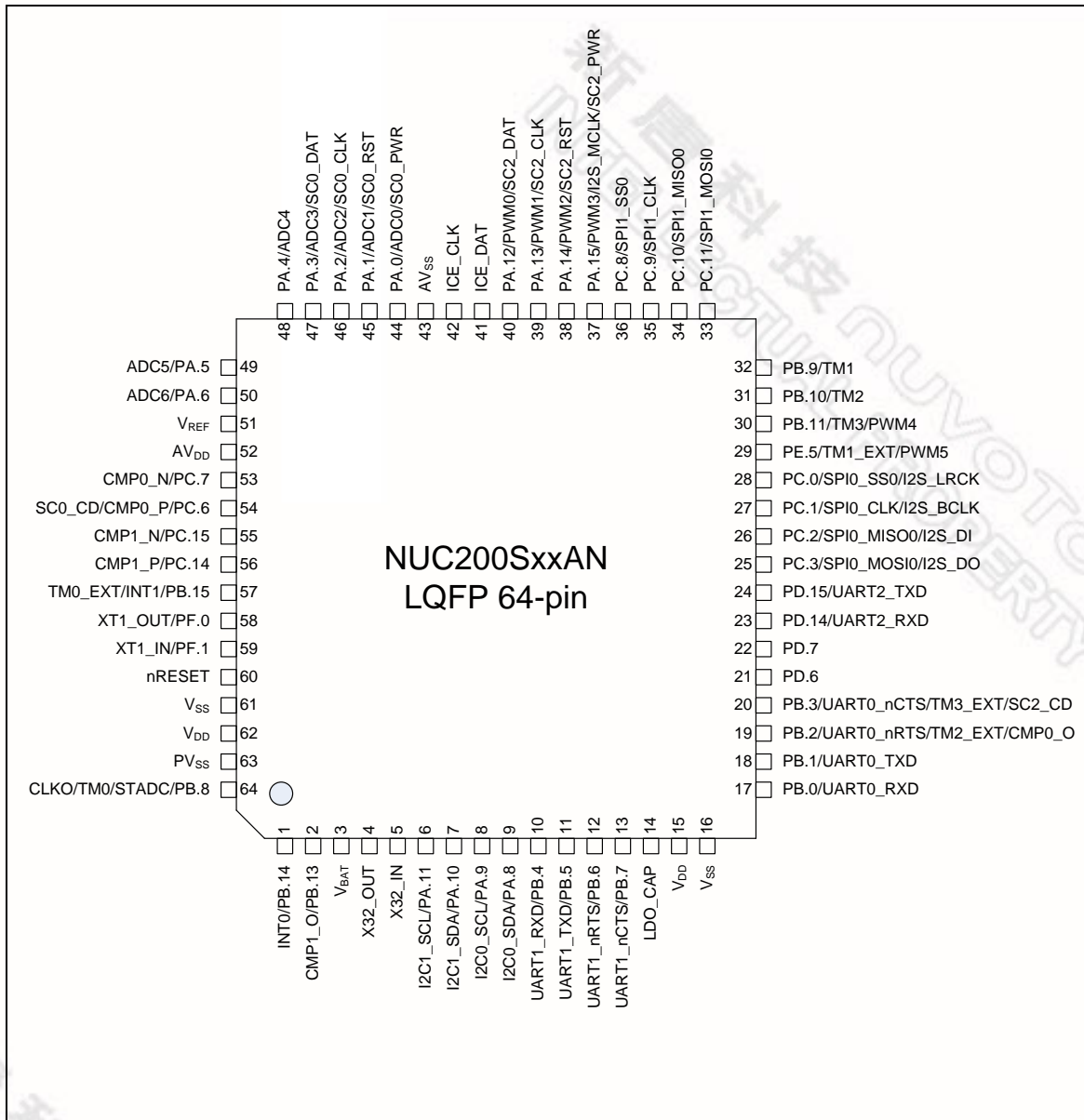


Figure 3-3 NuMicro™ NUC200SxxAN LQFP 64-pin Diagram



3.2.1.3 NuMicro™ NUC200LxxAN LQFP 48-pin

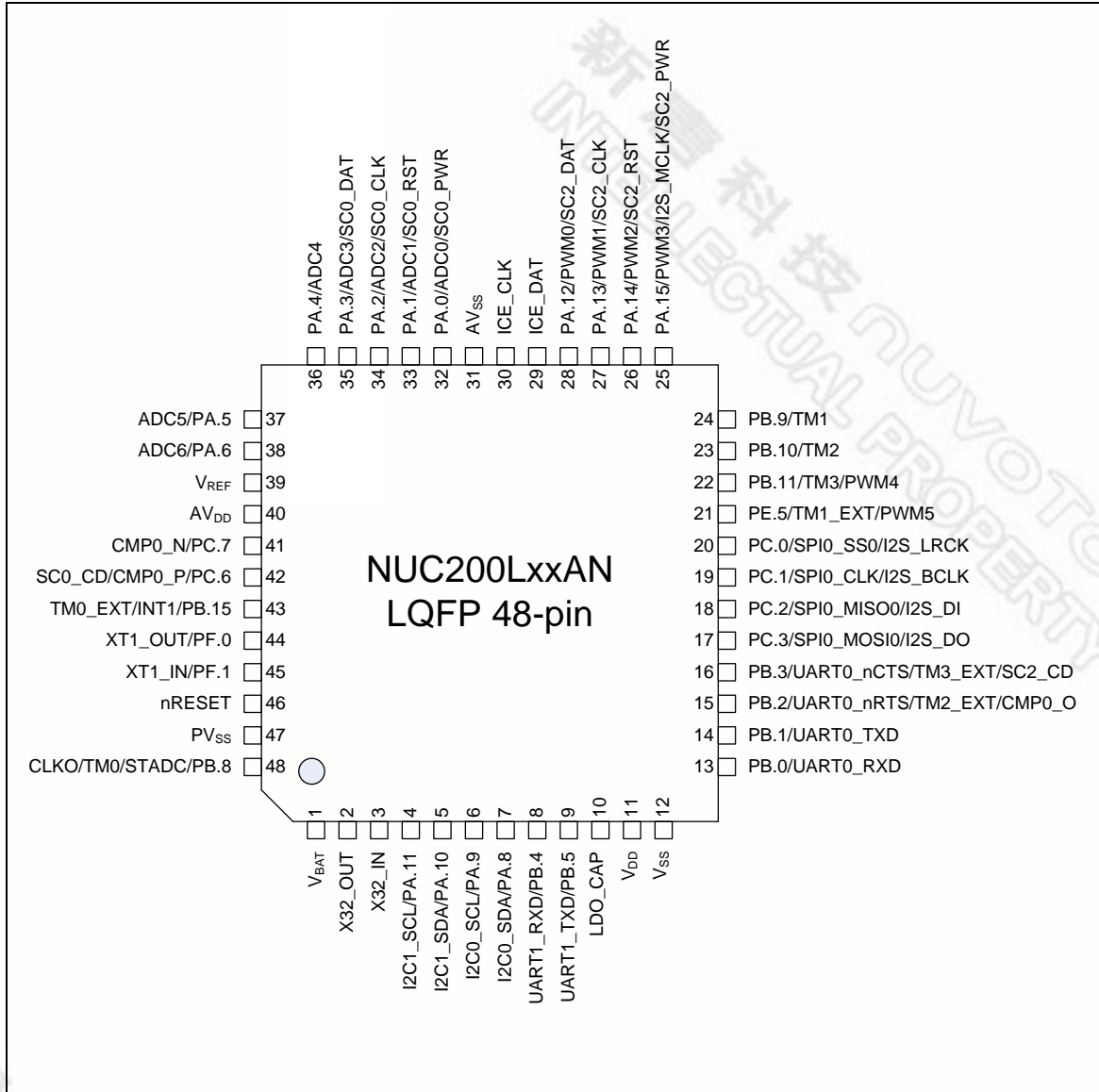


Figure 3-4 NuMicro™ NUC200LxxAN LQFP 48-pin Diagram

3.2.2 NuMicro™ NUC220 Pin Diagram

3.2.2.1 NuMicro™ NUC220VxxAN LQFP 100-pin

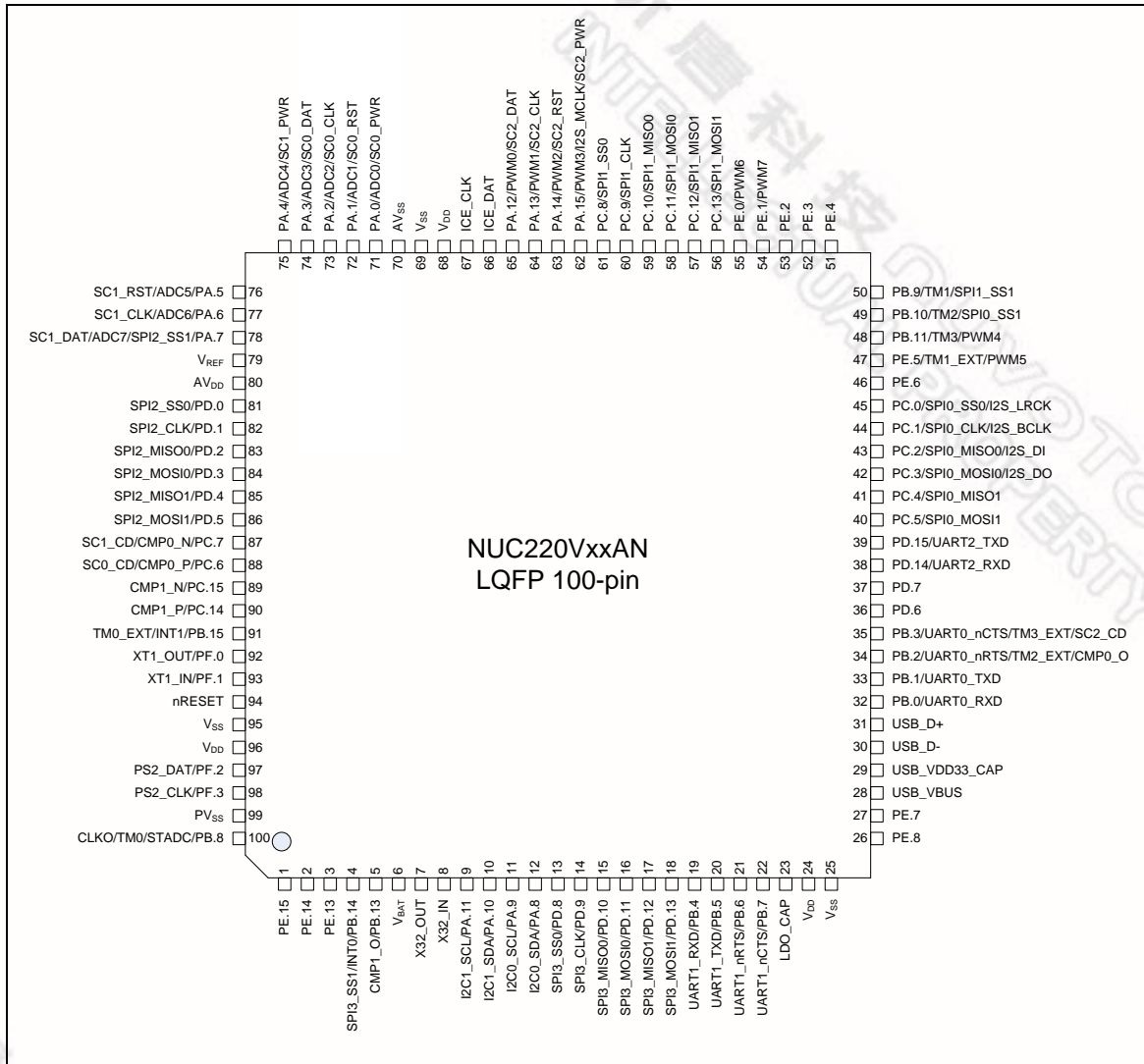


Figure 3-5 NuMicro™ NUC220VxxAN LQFP 100-pin Diagram

3.2.2.2 NuMicro™ NUC220RxxAN LQFP 64-pin

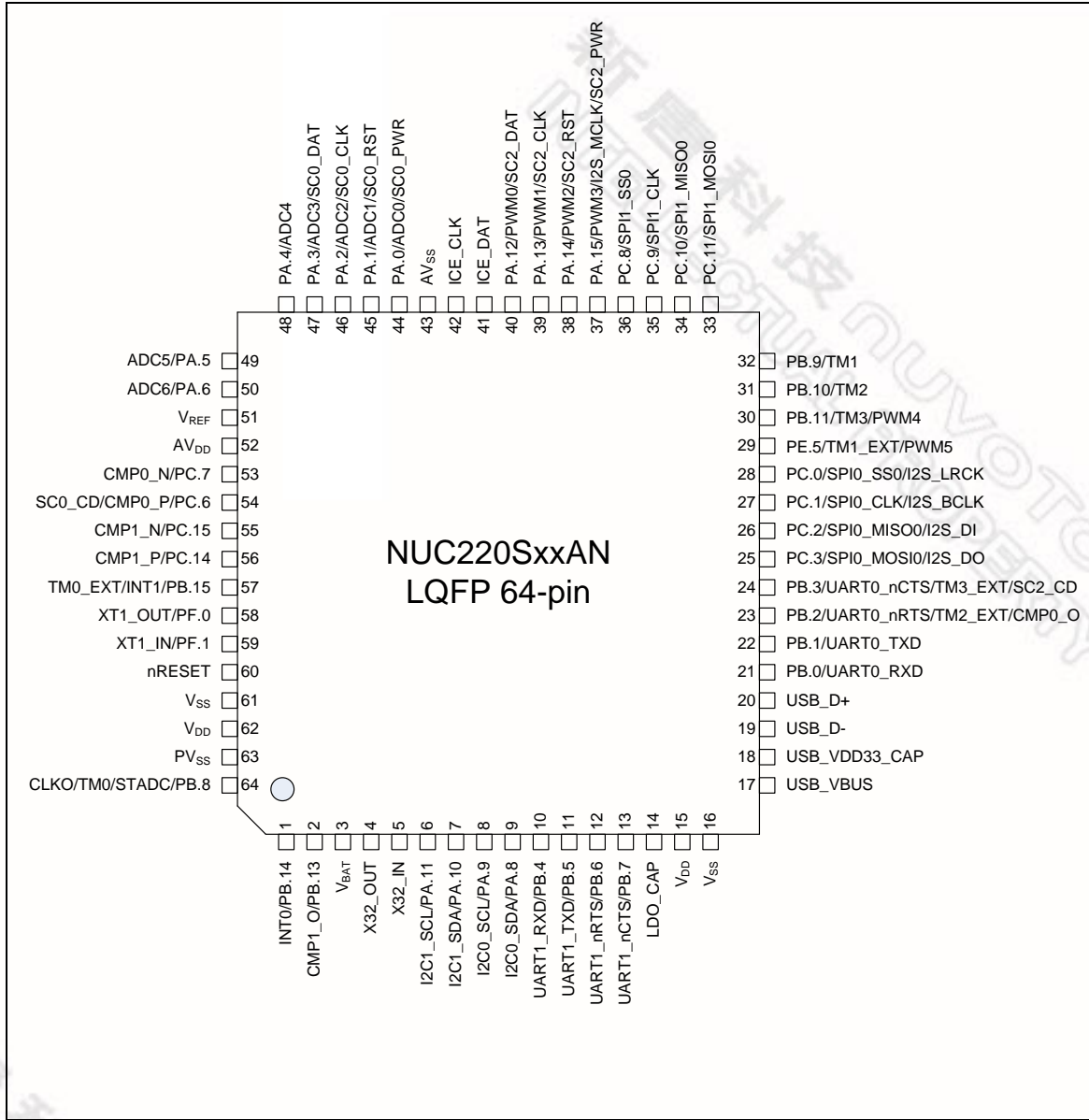


Figure 3-6 NuMicro™ NUC220SxxAN LQFP 64-pin Diagram

3.2.2.3 NuMicro™ NUC220LxxAN LQFP 48-pin

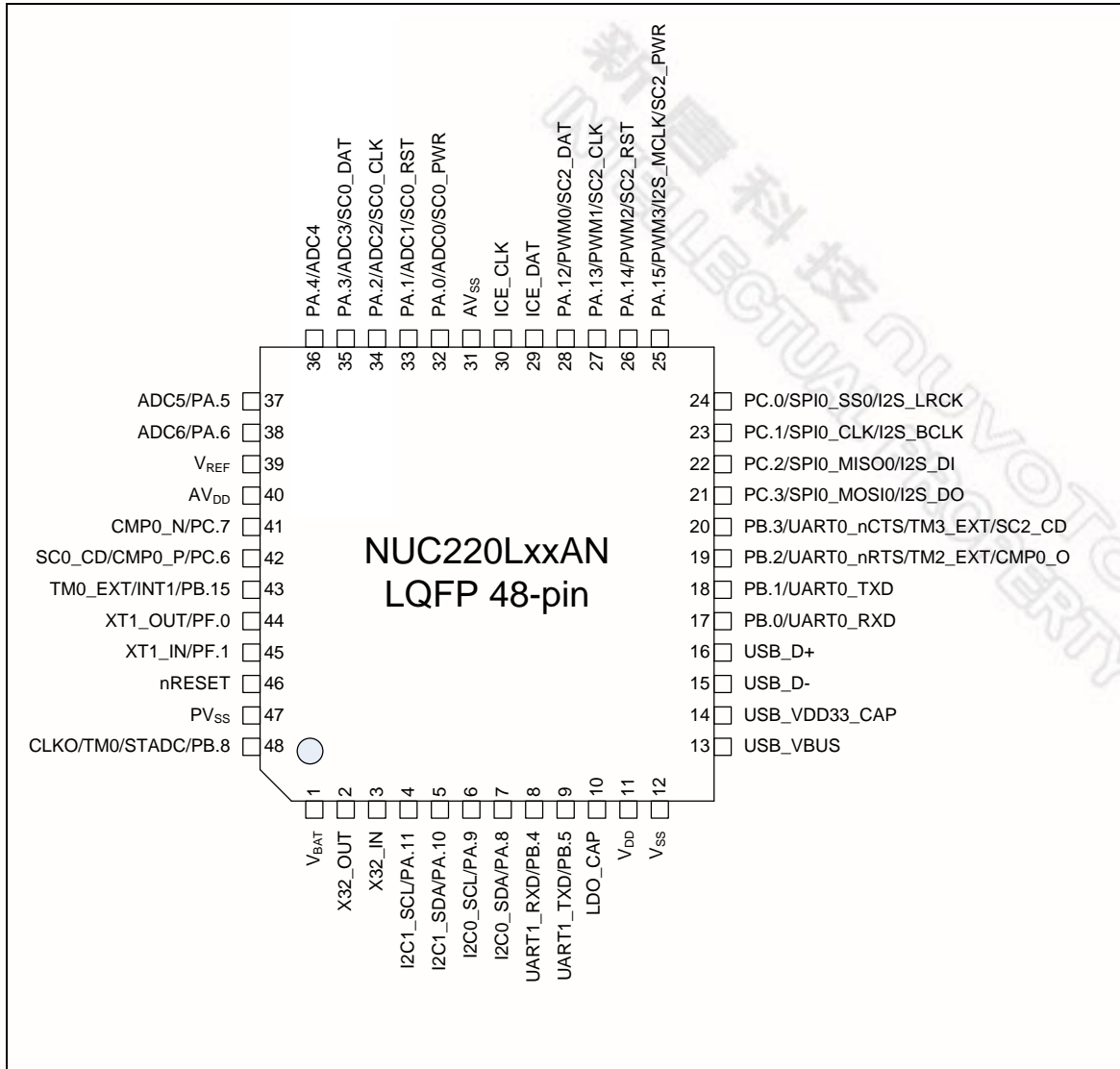


Figure 3-7 NuMicro™ NUC220LxxAN LQFP 48-pin Diagram

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC200 Block Diagram

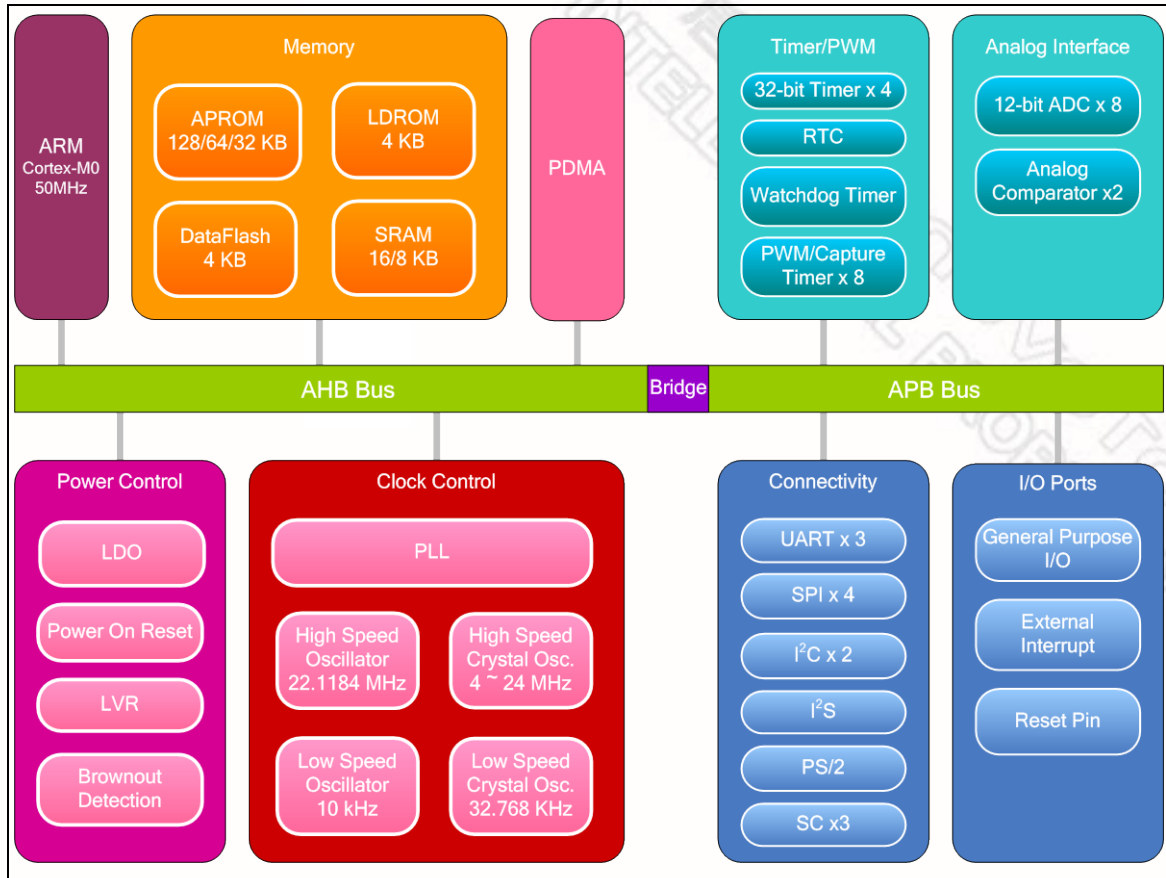


Figure 4-1 NuMicro™ NUC200 Block Diagram

4.2 NuMicro™ NUC220 Block Diagram

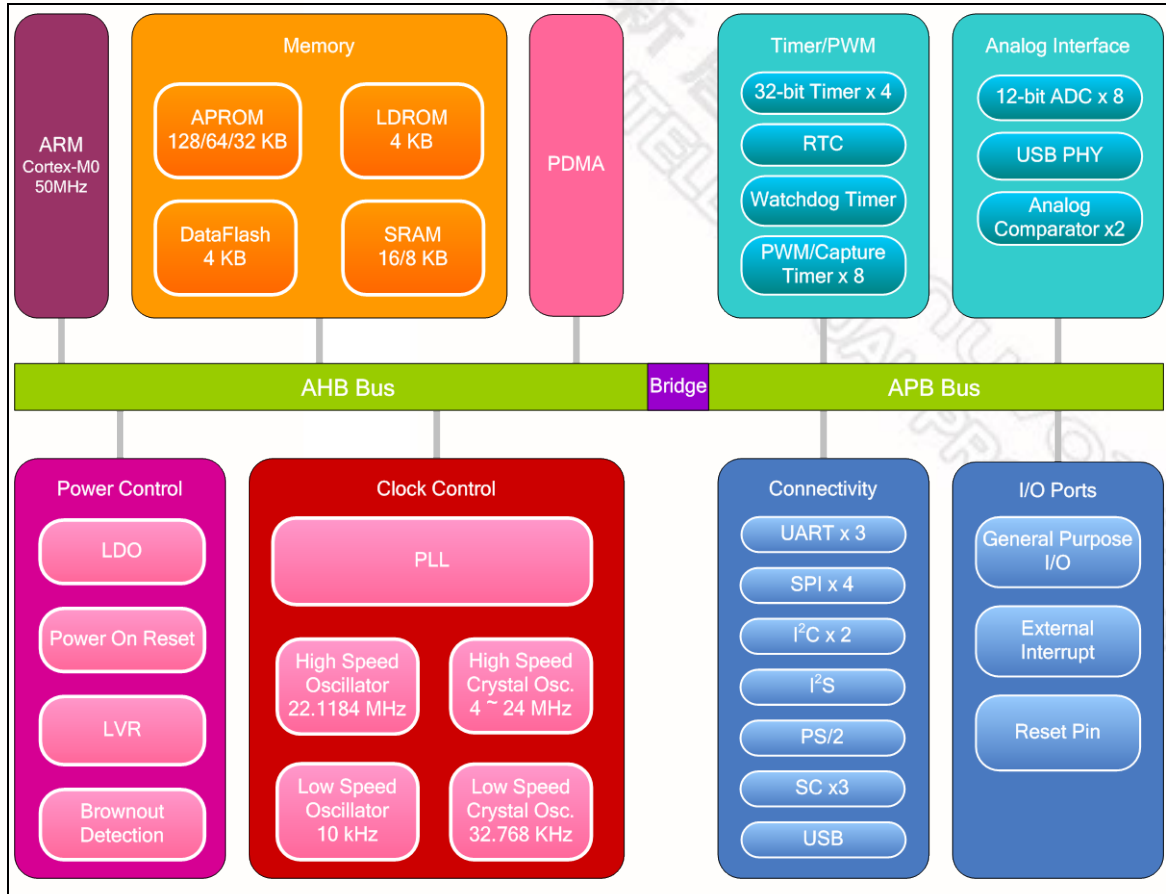
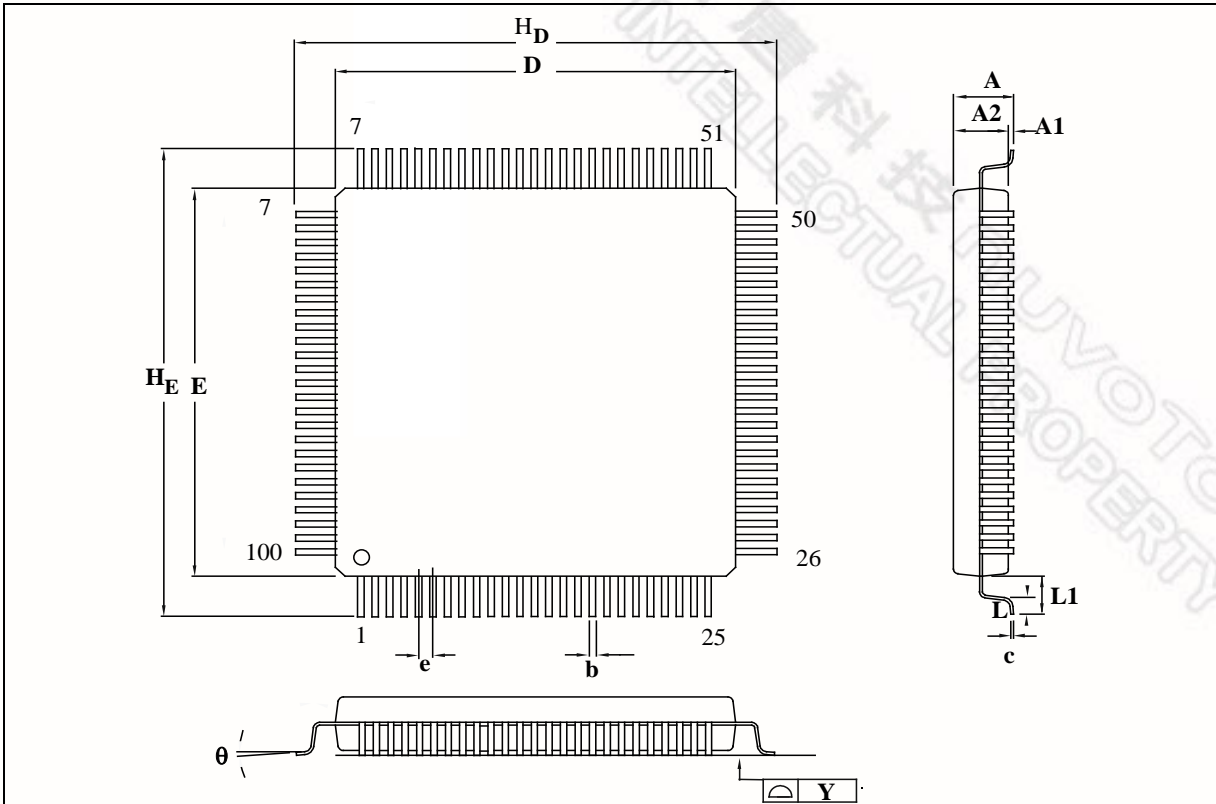


Figure 4-2 NuMicro™ NUC220 Block Diagram



5 PACKAGE DIMENSIONS

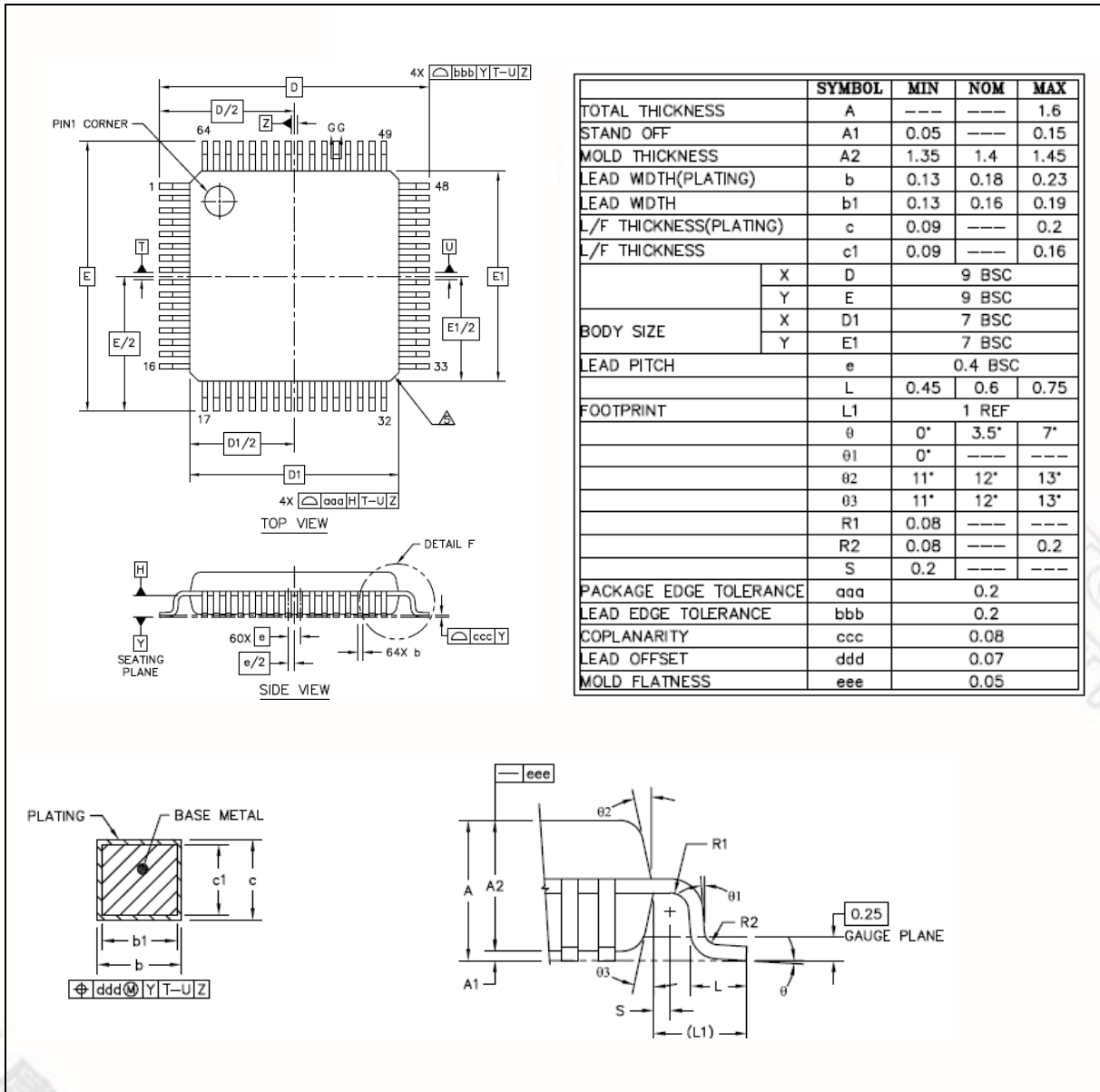
5.1 100-pin LQFP (14x14x1.4 mm footprint 2.0 mm)



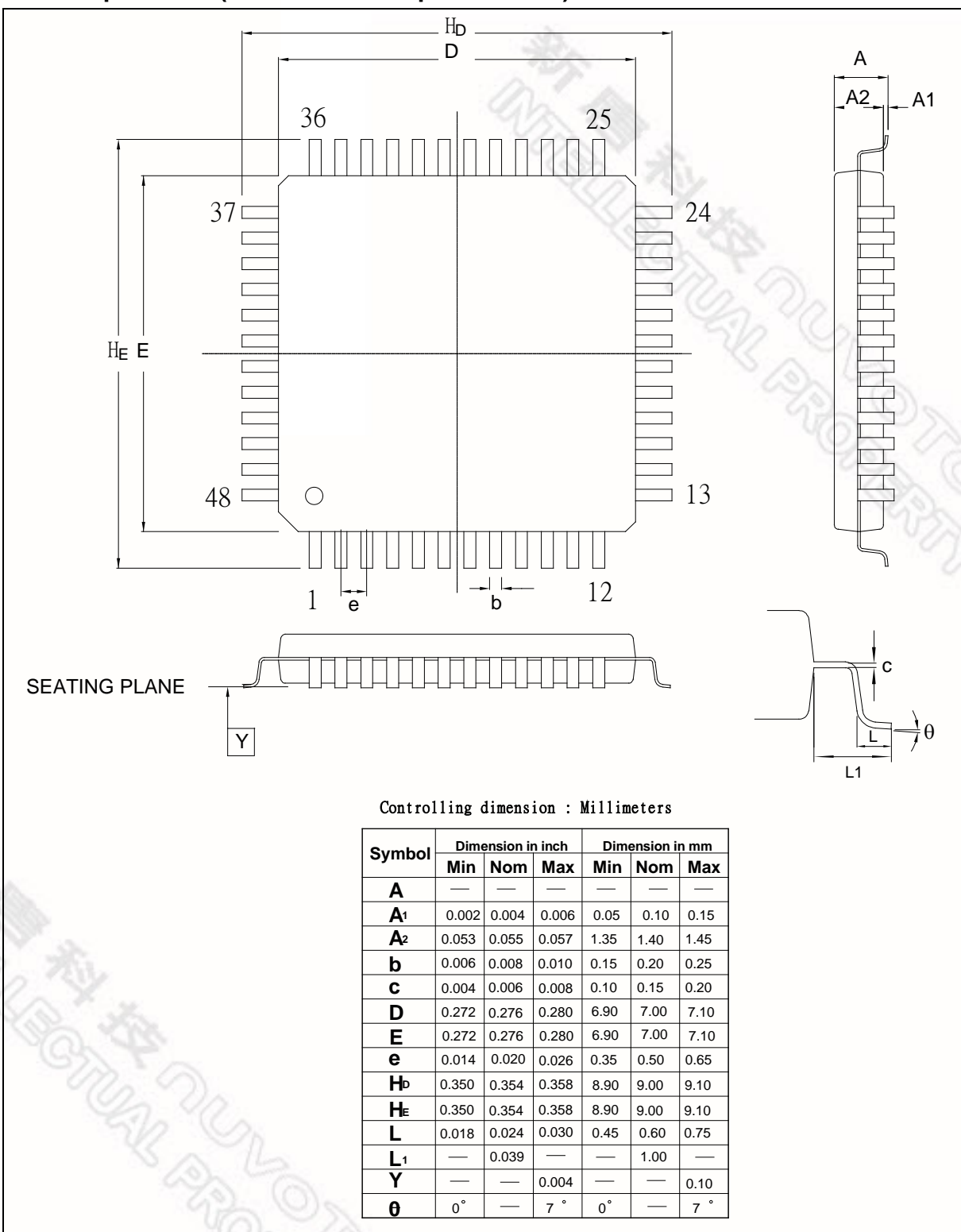
Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

5.2 64-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



5.3 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



6 REVISION HISTORY

REVISION	DATE	DESCRIPTION
V1.00	June 06, 2014	1. Initial release

Important Notice

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