AT24CSW01 and AT24CSW02 Series

I²C-Compatible (2-Wire) Serial EEPROM with a Security Register and Software Write Protection

1-Kbit (128 x 8) and 2-Kbit (256 x 8)

DATASHEET

Features

- Low-voltage Operation
  - V_{CC} = 1.7V to 3.6V
- Internal Organization:
  - 128 x 8 (1-Kbit, 128 byte)
  - 256 x 8 (2-Kbit, 256 byte)
- I²C-Compatible (2-Wire) Serial Interface
  - 100kHz Standard Mode, 1.7V to 3.6V
  - 400kHz Fast Mode (FM), 1.7 to 3.6V
  - 1MHz Fast Mode Plus (FM+), 1.7V to 3.6V
- Software Write Protection of the EEPROM Array
  - Five configuration options
  - Protection settings can be made permanent
- 256-bit Security Register
  - Unique, factory-programmed, 128-bit Serial Number in the first 16 bytes
    - Permanent read-only value
    - Guaranteed unique across entire CS Series of Serial EEPROMs
  - Additional 16 bytes of free user EEPROM provided to store critical user data
    - Can be made permanently read-only with a simple software sequence
    - Ideal for applications that need to protect critical or sensitive application data
- Factory Set Hardware Slave Address
  - Unique ordering code for each available slave address value (AT24CSW01x/02x)
- Ultra Low Active Current (1mA max) and Standby Current (0.8µA max)
- 8-byte Page Write Mode
  - Partial Page Writes and single Byte Write support included
- Self-timed Write Cycle (5ms max)
- High-reliability Device
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Green Package Options (Lead-free/Halide-free/RoHS-compliant)
  - 4-ball Ultra-Thin WLCSP

Description

The Atmel® AT24CSW01 and AT24CSW02 Device Family Series provides 1,024 / 2,048 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 128 / 256 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

The device features a Software Write Protection feature with five different programmable levels of protection for the EEPROM array. The protection settings of the device can made permanent if desired. Safeguards are included to prevent accidental invocation of the permanent feature.

Additionally, each device includes a Security Register with an extra 256 bits of EEPROM beyond the nominal EEPROM array. The Security Register is comprised of a read-only section of 16 bytes and an additional user-programmable section of 16 bytes.

The Security Register begins with a read-only section that contains a factory programmed guaranteed unique 128-bit Serial Number. The time consuming step of performing and ensuring true serialization of a product on a manufacturing line can be removed from the production flow by employing a CS Series Serial EEPROM. The 128-bit Serial Number is programmed and permanently locked from future writing during the Atmel production process. Further, this 128-bit location does not consume any of the user read/write area of the 1-Kbit / 2-Kbit Serial EEPROM. The uniqueness of the Serial Number is guaranteed across the entire CS Series of Serial EEPROMs regardless of the size of the memory array or the type of interface protocol. This means that as an application's needs for memory size or interface protocol evolve in future generations, any previously deployed Serial Number from any Atmel CS Series Serial EEPROM part will remain valid.

Following the 128-bit read-only Serial Number in the Security Register is an additional 16 bytes of EEPROM organized as 2 pages of 8 bytes each. This region of the Security Register is user-programmable, and if so desired, can later be permanently write protected with a software sequence. This user-programmable section of the Security Register is ideal for applications that need to irreversibly protect critical or sensitive application data.

The AT24CSW01x/02x is available in a best-in-class 4-ball Ultra-Thin WLCSP package and is accessed via an I^2C-compatible 2-wire serial interface. Other package options are available upon request. The device operates with a supply voltage ranging from 1.7V to 3.6V.

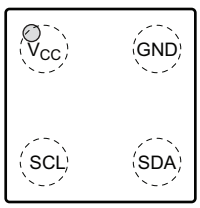
Table of Contents

1. Pin Descriptions and Pinouts

Table 1-1. Pin Descriptions

Pin Symbol	Pin Name and Functional Description	Asserted State	Pin Type
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power
SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 10KΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/ Output
SCL	**Serial Clock:** The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.	—	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power

4-ball WLCSP
(4U-13 Package Code)



Top View, Marking Side

Note: Drawing is not to scale.

2. Device Block Diagram

Figure 2-1. Block Diagram

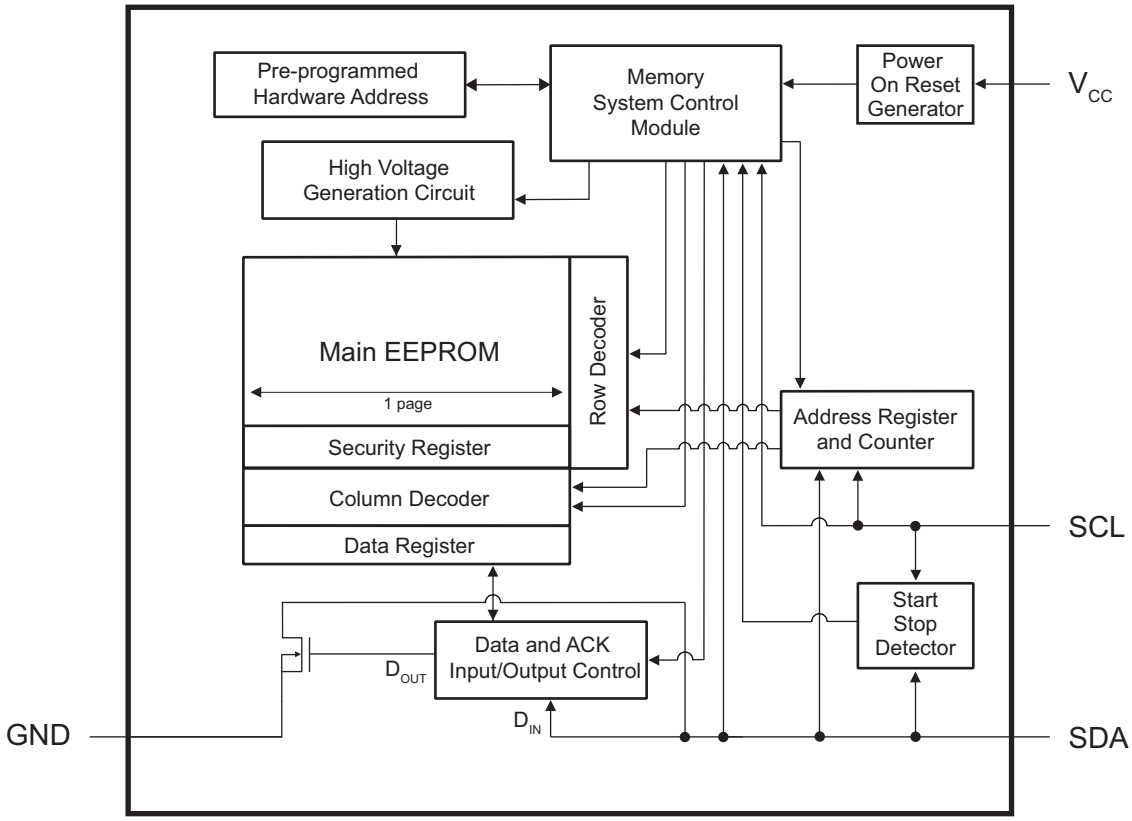
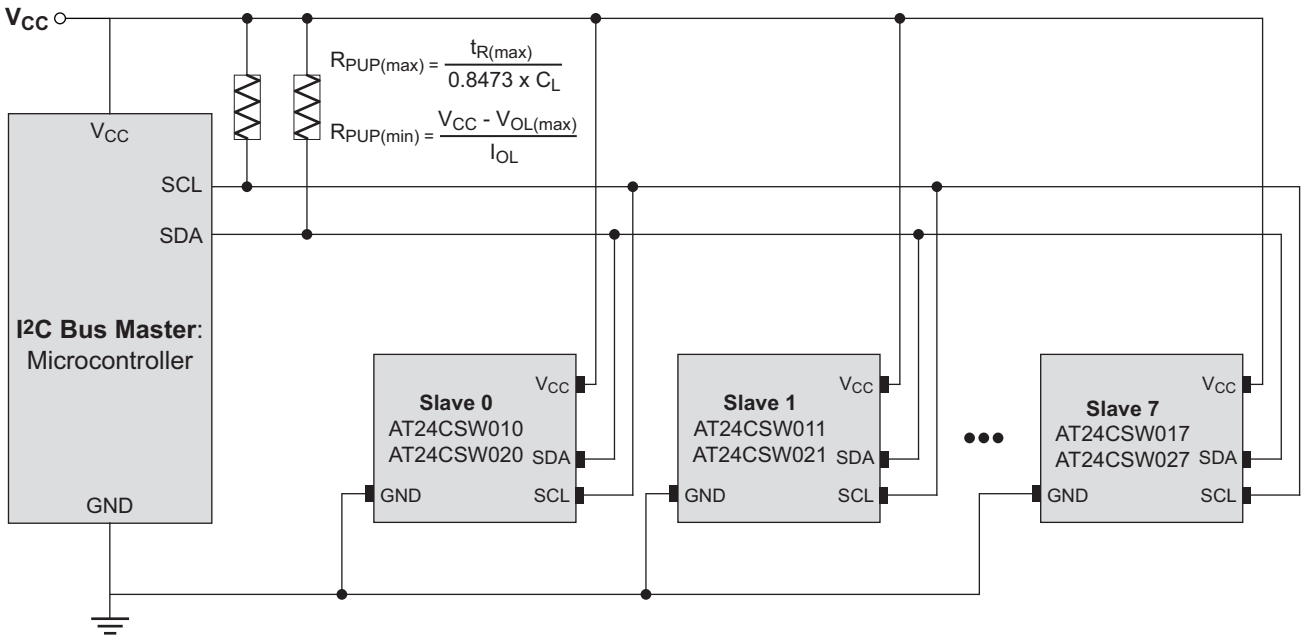


Figure 2-2. System Configuration Using 2-Wire Serial EEPROMs



3. Device Operation and Communication

The AT24CSW01x/02x operates as a slave device and utilizes a simple I^2C-compatible 2-wire digital serial interface to communicate with a host controller commonly referred to as the bus Master. The Master initiates and controls all read and write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master, as well as send data back to the Master. Data is always latched into the AT24CSW01x/02x on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pins incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During bus communication, one data bit is transmitted every clock cycle and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during the ninth clock cycle (ACK/NACK clock cycle) generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic-high state at the same time.

3.1 Clock and Data Transition Requirements

The SDA pin is an open drain terminal and therefore must be pulled high with an external pull-up resistor. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.

Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

The relationship of the AC timing parameters with respect to SCL and SDA for the AT24CSW01x/02x are shown in the timing waveform in Figure 10-1, "Bus Timing" on page 27. The AC timing characteristics and specifications are outlined in Figure 10.4, "AC Characteristics" on page 27.

3.2 Start and Stop Conditions

3.2.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable Logic 1 state and will bring the device out of standby mode. The Master uses a Start condition to initiate any data transfer sequence, therefore every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Please refer to Figure 3-1 for more details.

3.2.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master can use the Stop condition to end a data transfer sequence with the AT24CSW01x/02x, which will subsequently return to standby mode. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master will perform another operation. Please refer to Figure 3-1 for more details.

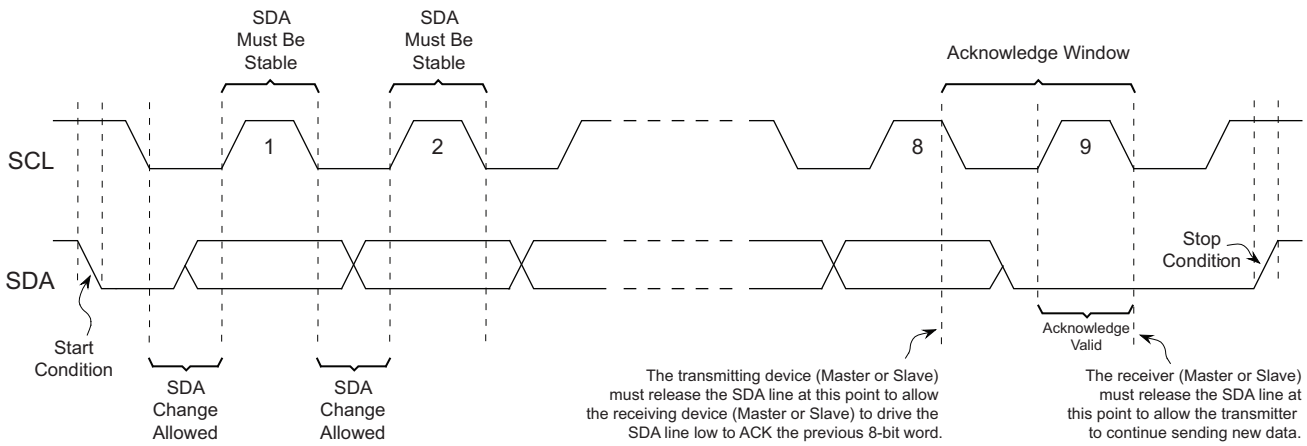
3.3 Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the Master that it has successfully received the data byte by responding with an ACK. An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a Logic 0 during the entire high period of the ninth clock cycle.

When the AT24CSW01x/02x device is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a Logic 1 response to the AT24CSW01x/02x instead of an ACK response during the ninth clock cycle. This is a NACK and is accomplished by the Master sending a Logic 1 during the ninth clock cycle, at which point the AT24CSW01x/02x will release the SDA line so the Master can then generate a Stop condition.

The transmitting device, which can be the bus Master or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle in order to allow the receiving device to drive the SDA line to a Logic 0 to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram below has been provided to better illustrate these requirements.

Figure 3-1. Start Condition, Data Transitions, Stop Condition and Acknowledge



The relationship of the AC timing parameters with respect to SCL and SDA for the AT24CSW01x/02x are shown in the timing waveform Figure 10-1 on page 27. The AC timing characteristics and specifications are outlined in Section 10.4 “AC Characteristics” on page 27.

3.4 Standby Mode

The AT24CSW01x/02x features a low power standby mode which is enabled when any one of the following occurs:

- A valid power-up sequence is performed (Section 10.5, “Power-Up Requirements and Reset Behavior”).
- A Stop condition is received by the devices unless it initiates an internal write cycle (Section 5., “Write Operations”).
- At the completion of an internal write cycle (Section 5., “Write Operations”).
- An unsuccessful match of the device type identifier or hardware address in the Device Address byte occurs (Section 4.1, “Device Addressing”).
- The bus Master does not ACK the receipt of data read out from the device; instead it sends a NACK response (Section 5., “Write Operations”).

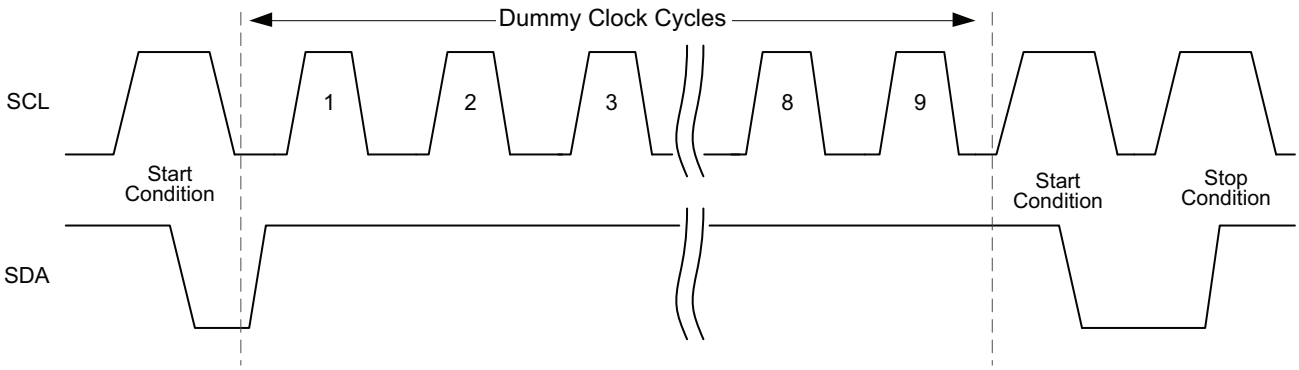
3.5 Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by a Stop condition as seen in Figure 3-2.

The device will be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Section 10.5.1 “Device Reset”).

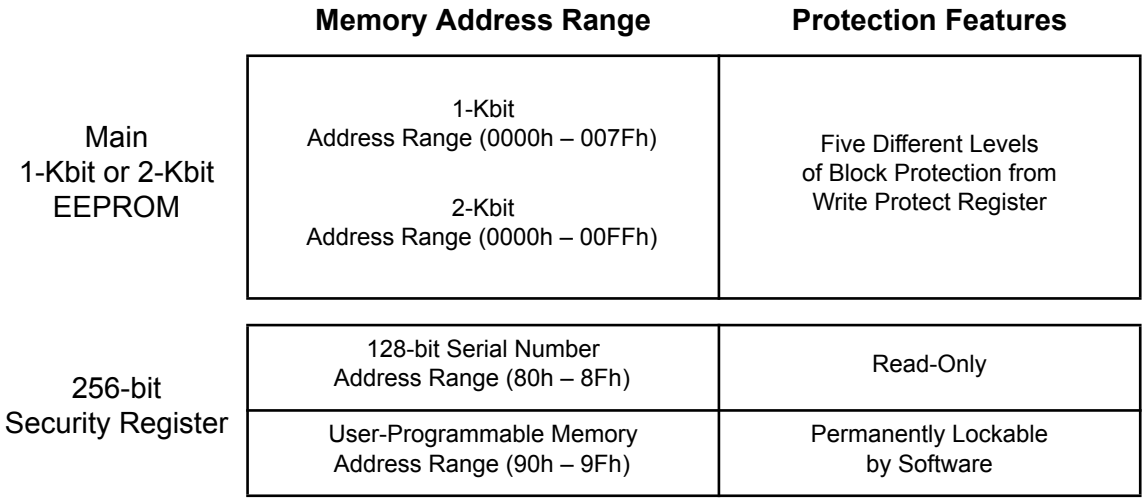
Figure 3-2. Software Reset



4. Memory Organization

The AT24CSW01x is internally organized as 16 pages of 8 bytes each and the AT24CSW02x is organized as 32 pages of 8 bytes each for the EEPROM Array. The device also contains a 32-byte Security Register which is organized as four pages of eight bytes each.

Figure 4-1. Memory Organization



The AT24CSW01x/02x also contains an 8-bit Write Protect Register that controls which regions of the memory can be written to. Details about how to use this register can be found in Section 6., “Write Protection”.

4.1 Device Addressing

4.1.1 Main 1-Kbit / 2-Kbit EEPROM Access

Accessing the device requires an 8-bit Device Address preceeded by a Start condition to enable the device for a read or write operation. Since multiple slave devices can reside on the same serial bus, each slave device must have its own unique address so that the Master can access each device independently.

The most significant four bits of the Device Address word is referred to as the Device Type Identifier. The Device Type Identifier `1010b` (Ah) is required in bits seven through four of the Device Address byte (Table 4-2.)

Following the 4-bit device type identifier are the slave address bits, A_2, A_1, and A_0. The value that the AT24CSW01x/02x will ACK to is preprogrammed in each device. Unique ordering codes are available for each of the eight possible slave combinations. The slave address preprogrammed in the device is embedded in the base part number as shown in Table 4-1 below. Full ordering code variations are shown in Section 11.1, “Ordering Code Detail”.

Table 4-1. Hardware Address Response by Part Number Series

Part Number Series		Hardware Address Bits		
1-Kbit	2-Kbit	A_2	A_1	A_0
AT24CSW01**0**	AT24CSW02**0**	0	0	0
AT24CSW01**1**	AT24CSW02**1**	0	0	1
AT24CSW01**2**	AT24CSW02**2**	0	1	0
AT24CSW01**3**	AT24CSW02**3**	0	1	1

Part Number Series		Hardware Address Bits		
1-Kbit	2-Kbit	A_2	A_1	A_0
AT24CSW01**4**	AT24CSW02**4**	1	0	0
AT24CSW01**5**	AT24CSW02**5**	1	0	1
AT24CSW01**6**	AT24CSW02**6**	1	1	0
AT24CSW01**7**	AT24CSW02**7**	1	1	1

The eighth bit of the Device Address (bit 0) is the Read/write Operation Select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.

Upon the successful comparison of the Device Address byte, the EEPROM will return an ACK. If a valid comparison is not made, the device will NACK and return to a standby state.

4.1.2 Security Register and Write Protect Register Access

The AT24CSW01x/02x contains a 32-byte Security Register, organized as 4 pages of 8 bytes each. This register contains a factory programmed guaranteed unique 128-bit Serial Number in the lower 16 bytes. The upper 16 bytes are user-programmable and can (later) be permanently write protected (see Section 8.3.1, “Lock Command”).

Access to this memory location is similar to the EEPROM region with the exception that the Device Address word must begin with 1011b (Bh). The behavior of the hardware address bits (A_2, A_1, A_0) remains the same as during a EEPROM addressing sequence (see Table 4-1 and Section 11.1, “Ordering Code Detail”).

The eighth bit of the Device Address (bit 0) is the Read/Write Operation Select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low. These bit positions have been summarized in Table 4-2.

While the lower order 16 bytes of the Security Register are read-only, the device will ACK if this bit is a Logic 0.

Warning: Accessing the Security Register is only possible if any sequence or command to the EEPROM (if one has been sent) has been properly terminated with a NACK or Stop condition from the Master. Without proper termination of that previous sequence, all communications with the Security Register will not execute successfully.

To read from the Security Register, please refer to Section 8.2, “Read Operations in the Security Register”, and for writing refer to Section 8.3, “Write Operations in the Security Register”.

4.1.3 Device Address and Word Address Byte Requirements

Table 4-2 below shows the valid Device Address bytes, and Table 4-3 shows the valid Word Address bytes for the AT24CSW01x/02x.

Table 4-2. Device Address Byte

Memory Region	Device Type Identifier				Hardware Address Bit			Read/ Write
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM Array	1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$
Security Register and Write Protect Register	1	0	1	1	A_2	A_1	A_0	R/$\overline{W}$

For all operations except the Current Address Read, a Word Address byte must be transmitted to the device immediately following the Device Address byte. The Word Address byte contains the 7-bit (AT24CSW01x) or 8-bit (AT24CSW02x) Memory Array Word Address to specify which location in the EEPROM to start reading or writing. Please refer to Table 4-3 to review these bit positions.

When accessing the Security Register, it is required that the A7 and A6 bits of the Word Address be set to 10b respectively. These bits are at a higher order address range than what is needed to address the 32 byte space (A4 through A0). It is recommended that all address bits that fall outside the address range that do not have other requirements be a Logic 0.

Table 4-3. Word Address Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM Array	A7[1]	A6	A5	A4	A3	A2	A1	A0
Security Register	1	0	X	A4	A3	A2	A1	A0
Security Register Lock Function	0	1	1	0	X	X	X	X
Write Protect Register	1	1	X	X	X	X	X	X

Note: 1. The A7 bit falls outside of the addressable 1K range and is therefore a don't care value on an AT24CSW01x.

5. Write Operations

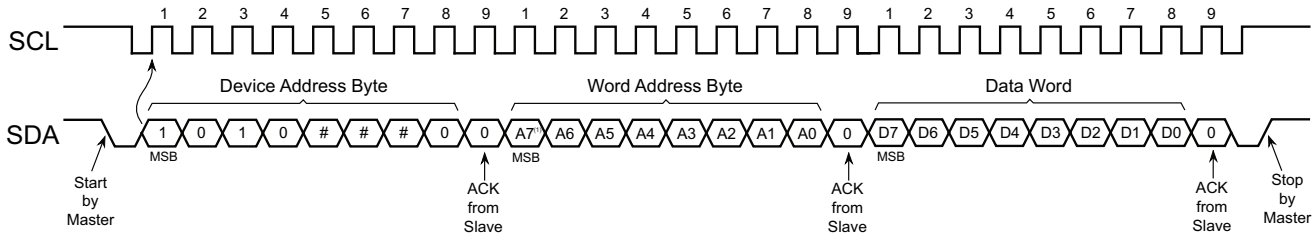
All AT24CSW01x/02x write operations begin with the Master sending a Start condition, followed by the appropriate Device Address byte with the R/W bit set to Logic 0, and then by the Word Address byte. The data value(s) to be written to the device immediately follows the Word Address bytes. When writing to a protected region, the device will ACK, but the internal write cycle will abort, leaving the device ready for a new operation.

5.1 Byte Write

The AT24CSW01x/02x supports the writing of a single 8-bit byte. Selecting a data word in the memory requires a 7-bit Word Address in the AT24CSW01x and an 8-bit Word Address in the AT24CSW02x.

Upon receipt of the proper Device Address and Word Address bytes, the EEPROM will send an ACK. The device will then be ready to receive an 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an ACK. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle which will be completed within t_{WR} (Section 5.4, “Write Cycle Timing”). While the data is being programmed into the Memory Array, all inputs are disabled during this write cycle and the EEPROM will not respond until the write cycle is complete.

Figure 5-1. Byte Write



Notes:
1. The A7 bit falls outside of the addressable 1K range and is therefore a don’t care value on an AT24CSW01x.
2. # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, “Ordering Code Detail”).

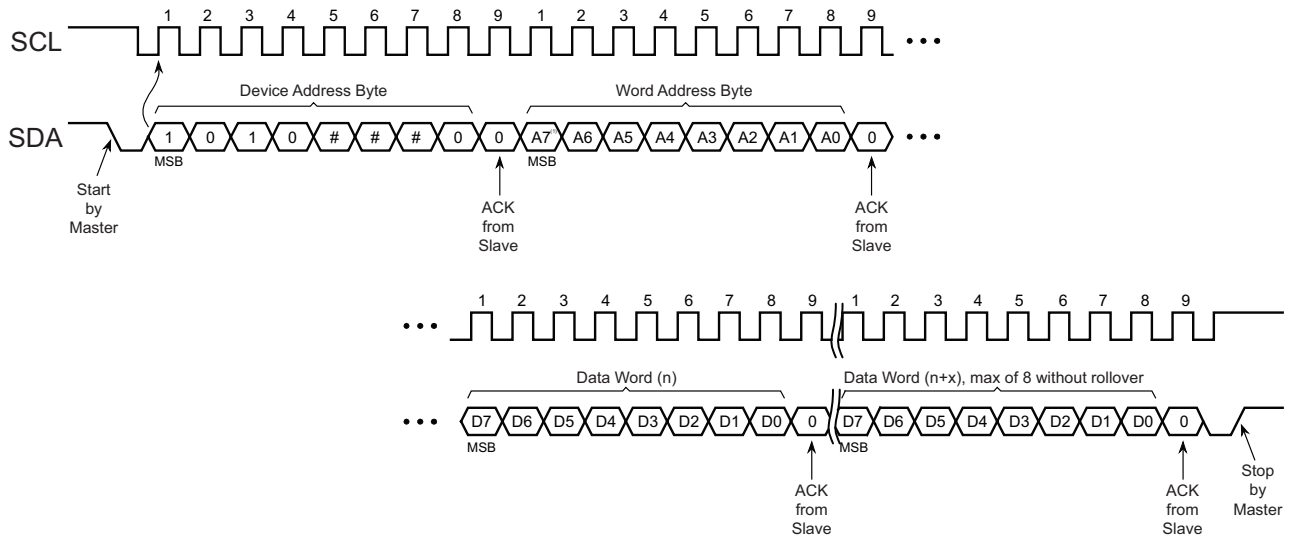
5.2 Page Write

A Page Write operation allows up to eight bytes to be written in the same write cycle provided that all bytes are in the same row of the Memory Array (where address bits A7/A6 through A3 are the same). Partial Page Writes of less than eight bytes are also allowed.

A Page Write is initiated the same way as a Byte Write, but the bus Master does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus Master can transmit up to seven additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written has been sent to the device, the bus Master must issue a Stop condition (see Figure 5-2) at which time the internally self-timed write cycle will begin.

The lower three bits of the Word Address are internally incremented following the receipt of each data word. The higher order address bits are not incremented and retain the memory page row location. Page Write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will “roll over” to the beginning of the same page. Nevertheless, creating a roll over event should be avoided as previously loaded data in the page could become unintentionally altered.

Figure 5-2. Page Write



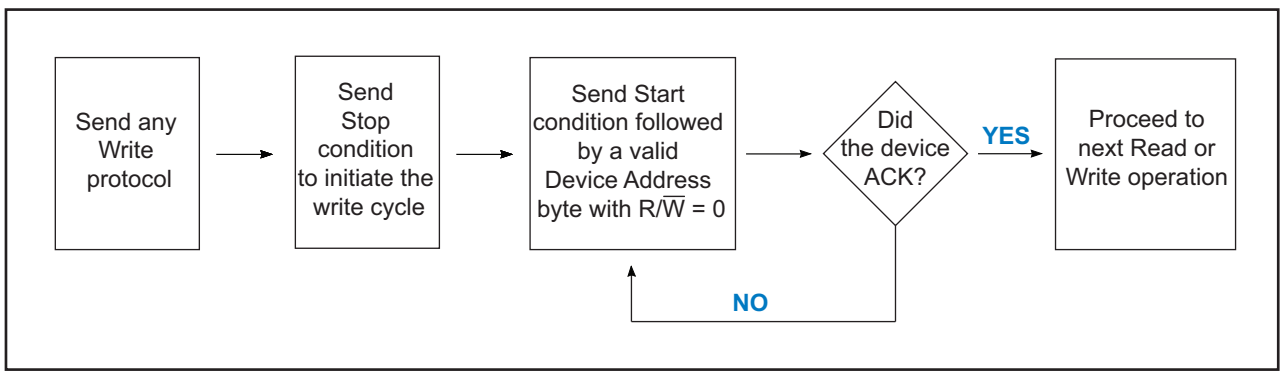
Notes: 1. The A7 bit falls outside of the addressable 1K range and is therefore a don't care value on an AT24CSW01x.
2. # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, "Ordering Code Detail").

5.3 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}). This method allows the application to know immediately when the Serial EEPROM write cycle has completed so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid Device Address byte with the R/$\overline{W}$ bit set at Logic 0. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new read or write operation to be immediately initiated. A flow chart has been included below in Figure 5-3 to better illustrate this technique.

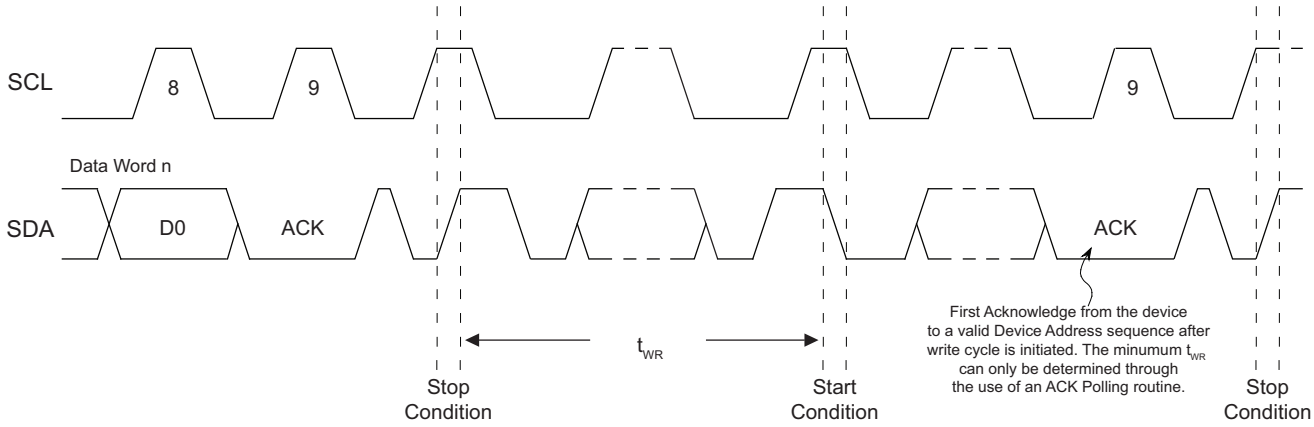
Figure 5-3. Acknowledge Polling Flow Chart



5.4 Write Cycle Timing

The length of the self-timed write cycle (t_{WR}) is defined as the amount of time from the Stop condition that begins the internal write operation to the Start condition of the first Device Address byte sent to the AT24CSW01x/02x that it subsequently responds to with an ACK. The figure below has been included to show this measurement. During the internally self-timed write cycle, any attempts to read or write to the memory array will not be processed.

Figure 5-4. Write Cycle Timing



6. Write Protection

6.1 Software Write Protection of the EEPROM Array

The AT24CSW01x/02x utilizes a software scheme that allows a portion or the entire EEPROM to be inhibited from being written to by modifying the contents of the Write Protection Register (WPR). If desired, the WPR can be set so that it may no longer be modified, thereby making the current protection scheme permanent.

The status of the WPR can be determined by following a Random Read sequence. Changing the state of the WPR is accomplished with a Byte Write sequence with the requirements outlined in this section.

Accessing the WPR requires the use of `1011b` (Bh) as the Device Type Identifier in the Device Address (see Table 6-1). Following the Device Type Identifier is the Hardware Address bits (A_2, A_1, A_0) for which the values are determined by the ordering code of the device (see Section 11.1, “Ordering Code Detail”). Finally, Bit 0 is the Read/Write select bit where a Logic 1 is used for reading and Logic 0 is used for writing.

Table 6-1. Device Address Byte Requirements for Accessing the Write Protect Register

Memory Region	Device Type Identifier				Hardware Address Bits			Read/ Write
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write Protect Register	1	0	1	1	A_2	A_1	A_0	R/$\overline{W}$

When accessing the Write Protect Register, it is required that the A7 and A6 bits of the Word Address be set to `11b` respectively. The remaining bits of the Word Address Byte are don’t care bits as depicted in Table 6-2 below.

Table 6-2. Word Address Byte Requirements for Accessing the Write Protect Register

	A7	A6	A5	A4	A3	A2	A1	A0
Write Protect Register	1	1	X	X	X	X	X	X

Following the Word Address byte are the contents of the 8-bit Write Protect Register. The register format is shown in Table 6-3, and the WPR bit functions are included in Table 6-4.

Table 6-3. Write Protect Register Format

	D7	D6	D5	D4	D3	D2	D1	D0
Read WPR	0	0	0	0	WPRE	WPB1	WPB0	WPRL
Write WPR	0	1	0: No Lock 1: Set Lock	0				

Write Protect Enable (WPRE): The Write Protect Enable Bit is used to enable or disable the device Software Write Protect. A Logic 0 in this position will disable Software Write Protection, and a Logic 1 will enable this function.

Write Protect Block Bits (WPB1:WPB0): The Write Protect Block bits allow four levels of protection of the Memory Array provided that the WPRE bit is a Logic 1. If the WPRE bit is a Logic 0, the state of the WPB1:0 bits have no impact to device protection. The protected address ranges are found in Table 6-5.

Write Protect Lock Bit (WPRL): The Write Protect Lock Bit is used to permanently lock the current state of the WPR. A Logic 0 indicates that the WPR can be modified, whereas a Logic 1 indicates the WPR has been locked and can no longer be modified. To safeguard against accidental locking of the WPR, the D5 bit must match the WPRL bit (D0 bit) sent to the device. If these bits do not match, the write cycle is aborted and the WPR contents are not modified.

Table 6-4. Write Protect Register Bit Function

Bit	Name		Type	Description	
3	WPRE	Write Protect Register Enable	R/W	0	No Software Write Protection enabled (*factory default*).
				1	Write protection is set by the state of the WPB[1:0] bits.
2:1	WPB1	Write Protect Block Bits	R/W	00	Upper quarter of EEPROM is write protected (*factory default*).
				01	Upper half of EEPROM is write protected.
	WPB0			10	Upper 3/4 of EEPROM is write protected.
				11	Entire EEPROM is write protected.
0	WPRL	Write Protect Lock Bit	R/OTP	0	WPR can be written to; requires D5 = 0 during write (*factory default*).
				1	WPR will become permanently locked (requires D5 = 1) during write.

6.1.1 Protected Address Ranges Set by WPB1 and WPB0

The EEPROM array in the AT24CSW01x/02x will be protected from writing in accordance with the WPB1 and WPB0 bit values as long as the WPRE bit is set to Logic 1. If the WPRE bit is set to Logic 0, no portion of the EEPROM array will be protected. The combination of these three bits creates five possible levels of protection for the device. The protected address ranges of the memory are shown in the table below.

Table 6-5. Word Address Byte Requirements for Accessing the Write Protect Register

Protection Level	WPRE	WPB1	WPB0	Protected Address Range		Unprotected Address Range	
				1-Kbit	2-Kbit	1-Kbit	2-Kbit
None	0	X	X	None	None	0h – 7Fh	0h – FFh
Upper Quarter	1	0	0	60h – 7Fh	C0h – FFh	0h – 5Fh	0h – BFh
Upper Half	1	0	1	40h – 7Fh	80h – FFh	0h – 3Fh	0h – 7Fh
Upper Three-Quarter	1	1	0	20h – 7Fh	40h – FFh	0h – 1Fh	0h – 3Fh
Full Array	1	1	1	0h - 7Fh	0h - FFh	None	None

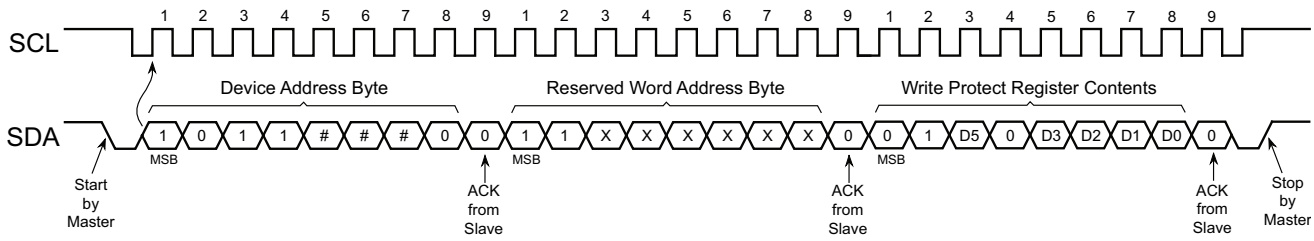
6.1.2 Writing to the Write Protect Register

When writing the WPR, data bit 7 through 4 are used to ensure that a write operation was intentional. For all write operations to the WPR, bit 6 must be a Logic 1 as seen in Table 6-3.

Additionally, data bit 5 must be set in accordance with the D0 bit value (WPRL) as noted below. If the WPR is to remain unlocked, then the upper nibble sent during the write sequence would be 4h and D0 must be a Logic 0, whereas if the WPR is to be permanently locked, the upper nibble would need to be 6h and D0 must be a Logic 1. A mismatch of D5 and the WPRL bit will cause the write cycle to abort.

Sending more than one byte to the AT24CSW01x/02x when trying to write to the WPR will cause the write cycle to abort and the contents of the WPR will not be changed. Additionally, if the WPR is already locked (WPRL = 1), the write cycle will not execute and the device will be ready for a new operation.

Figure 6-1. Write Protection Register Write Sequence



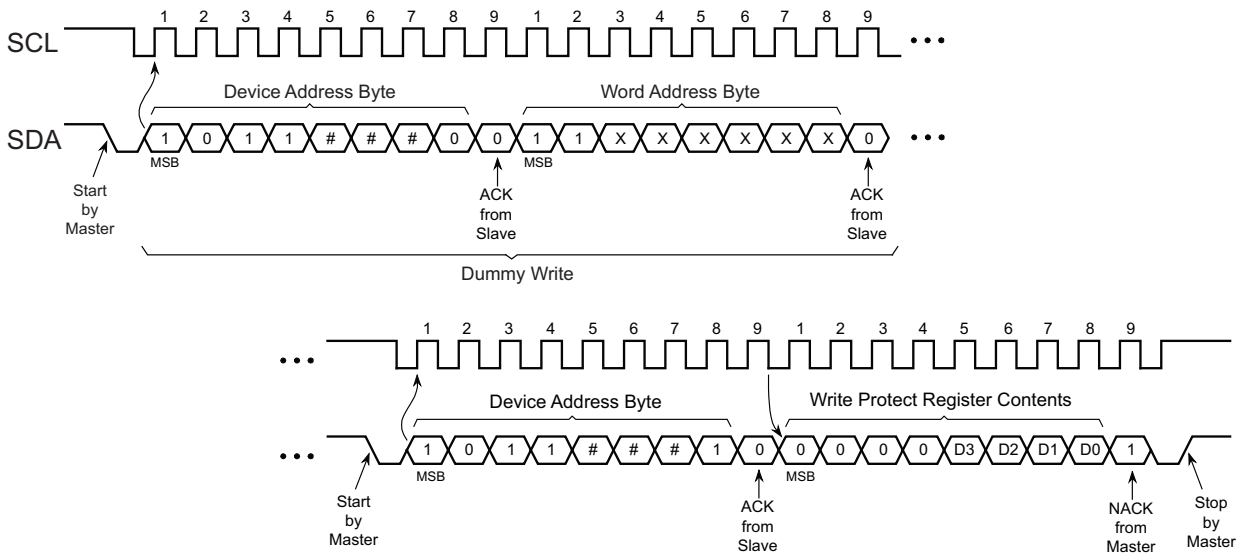
Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, “Ordering Code Detail”).

6.1.3 Reading the Write Protect Register

To read the contents of the Write Protect Register, a Random Read sequence must be sent to the device (see Section 7.2, “Random Read”) so that the reserved Word Address bits A7 and A6 can properly be set. It is not possible to read the contents of the WPR with a Current Address Read sequence.

When reading the WPR contents, data bit 7 through 4 will always read as a Logic 0 as seen in Table 6-3.

Figure 6-2. Read Write Protect Register Sequence



Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1).

7. Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write Select bit in the Device Address word must be a Logic 1. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

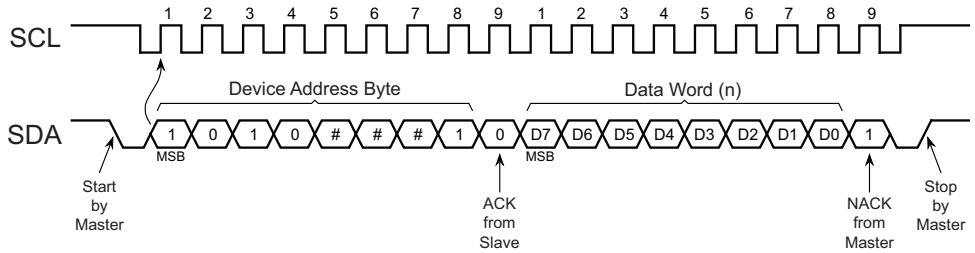
Warning: The AT24CSW01x/02x contains a single address pointer register, which is shared by both the EEPROM and the Security Register. As such, when changing from one region to the other, the first read operation in the new region should begin with a Dummy Write Sequence (i.e. a Random Read operation with the new region's Device Address and Word Address bytes) in order to ensure the address pointer is set to a known value. See Section 8.2, "Read Operations in the Security Register" for additional requirements on read operations in the Security Register.

7.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation incremented by one. This address stays valid between operations as long as the V_{CC} is maintained to the part. The address "roll over" during read is from the last byte of the last page to the first byte of the first page of the memory.

A Current Address Read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition followed by a valid Device Address byte with the R/$\overline{W}$ bit set to Logic 1. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of Read operations will be terminated if the bus Master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into standby mode. After the NACK response, the Master may send a Stop condition to complete the protocol or send a Start condition to begin the next sequence.

Figure 7-1. Current Address Read



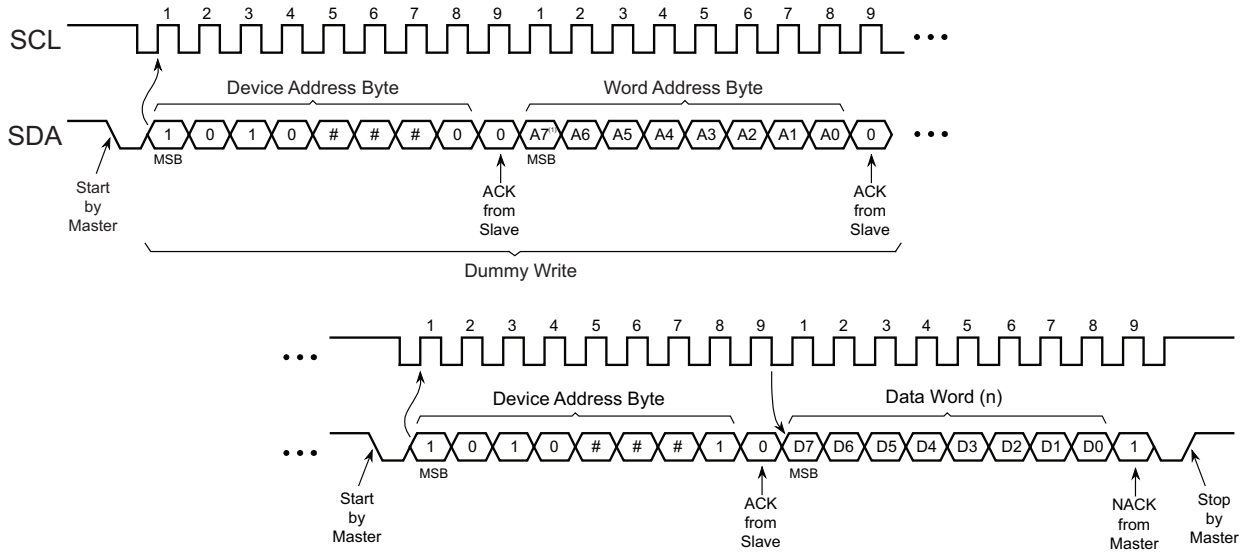
Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, "Ordering Code Detail").

7.2 Random Read

A Random Read begins in the same way as a Byte Write operation does to load in a new data Word Address. This is known as a “dummy write” sequence; however, the Stop condition of the Byte Write must be omitted to prevent the part from entering an internal write cycle. Once the Device Address and Word Address bytes are clocked in and acknowledged by the EEPROM, the bus Master must generate another Start condition. The bus Master now initiates a Current Address Read by sending a Start condition followed by a valid Device Address byte with the R/W bit set to Logic 1. The EEPROM will ACK the Device Address and serially clock out the data word on the SDA line. All types of read operations will be terminated if the bus Master does not respond with an ACK (it NACKs) during the ninth clock cycle which will force the device into standby mode. After the NACK response, the Master may send a Stop condition to complete the protocol, or send a Start condition to begin the next sequence.

Caution: When switching between the EEPROM and the Security Register, if the first operation is a read, then that operation needs to be a Random Read to ensure the address pointer is set to a known value.

Figure 7-2. Random Read

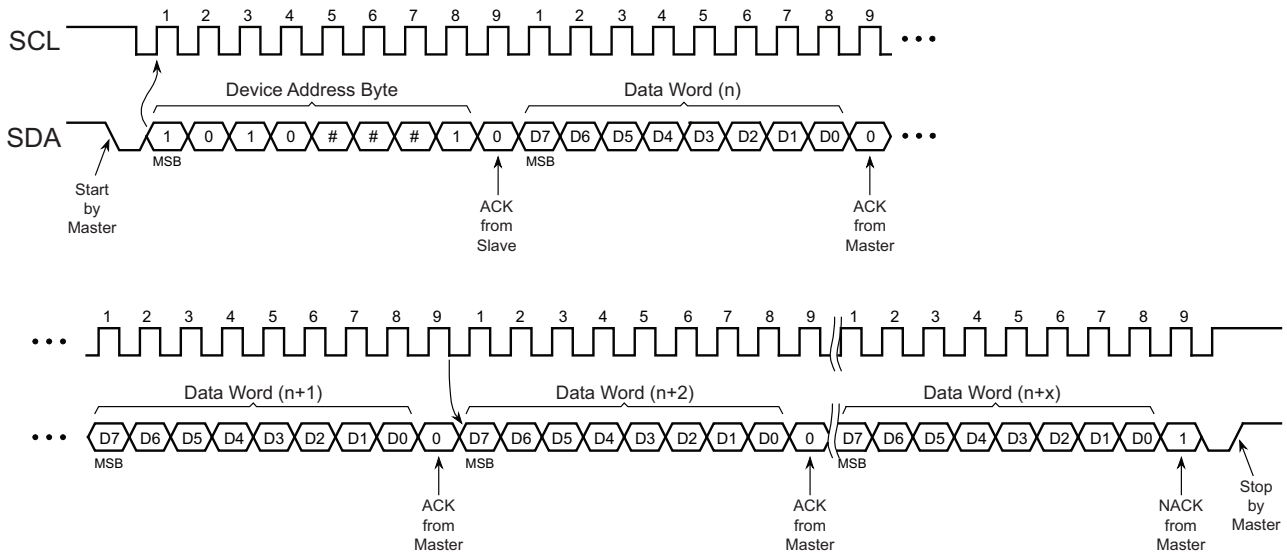


Notes: 1. The A7 bit falls outside of the addressable 1K range and is therefore a don’t care value on an AT24CSW01x.
2. # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, “Ordering Code Detail”).

7.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Read. After the bus Master receives a data word, it responds with an acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the data Word Address and serially clock out sequential data words. When the maximum memory address is reached, the data Word Address will "roll over" and the sequential read will continue from the beginning of the Memory Array. All types of read operations will be terminated if the bus Master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into standby mode. After the NACK response, the Master may send a Stop condition to complete the protocol or send a Start condition to begin the next sequence.

Figure 7-3. Sequential Read from a Current Address Read



Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, "Ordering Code Detail").

8. Security Register

The AT24CSW01x/02x includes a 32-byte Security Register. The Security Register is segmented into a 16-byte read-only section and a 16-byte user-programmable section organized as 4 pages of 8 bytes each. The user-programmable portion supports both Byte Write and Page Write operations. The read-only section contains a pre-programmed guaranteed unique 128-bit Serial Number. The user-programmable portion may be permanently locked at any time with the Lock command.

Table 8-1. Security Register Organization

Security Register Byte Number									
0	1	. . .	14	15	16	17	. . .	30	31
Atmel Factory Programmed (Read-only) 0 - 15: Device Serial Number					User Programmable (Lockable)				

8.1 Custom Programming Option

Atmel supports the pre-programming and subsequent locking of customer specific data in the user-programmable portion of the Security Register. Contact the local Atmel Sales representative for more details on this custom solution.

8.2 Read Operations in the Security Register

Random Read and Sequential Read operations are supported by the Security Register provided the Device Address uses a Device Type Identifier of `1011b` (Bh), and the A7 and A6 bits of the Word Address are set to `10b`. Current Address Reads in the Security Register are not supported due to the fact that the required A7 and A6 address bits in the Word Address byte do not get sent to the device.

The first 16 bytes of the Security Register are by definition read-only and contain a pre-programmed guaranteed unique 128-bit Serial Number. The remaining 16 bytes of the Security Register are user-programmable and can be locked from any future programming operations (see Section 8.3.1, “Lock Command” for more details).

8.2.1 Address Pointer Behavior

The AT24CSW01x/02x contains a single address pointer that is shared between the EEPROM and the Security Register. As such, any read operation to the Security Register should begin with a Dummy Write Sequence (i.e. Random Read) to ensure the address pointer is set to a known value. If the preceding operation was to the Security Register, the address pointer will retain the last access location incremented by one.

8.2.2 Serial Number Read

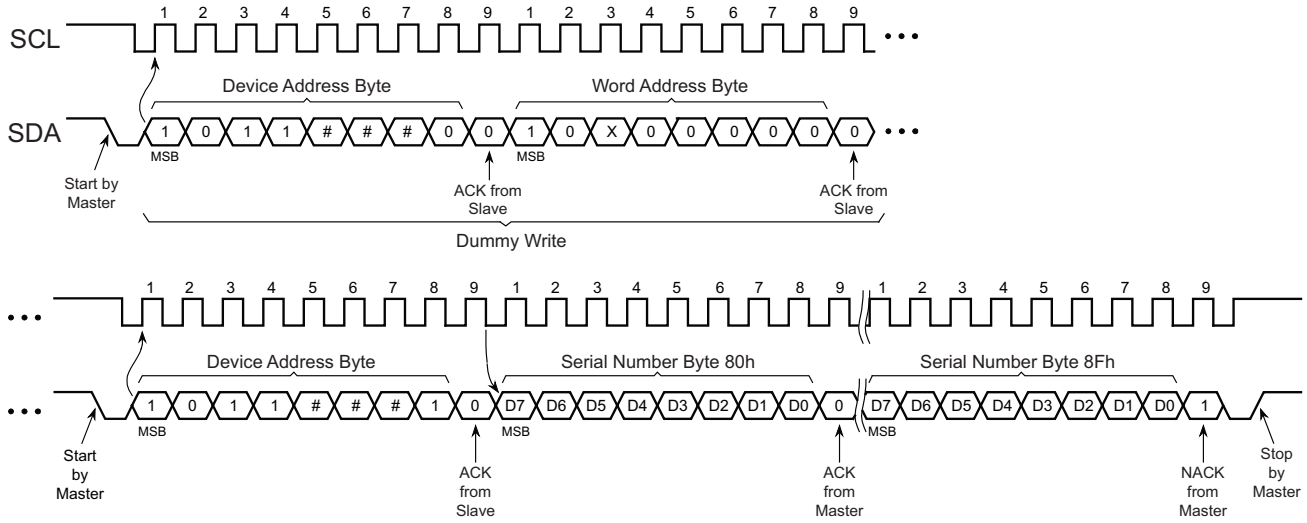
Reading the 128-bit Serial Number is similar to the Sequential Read sequence but requires use of the Device Address seen in Figure 8-1, a dummy write, and a specific Word Address. The Word Address must begin with a `10b` sequence regardless of the intended address. If a Word Address other than `10b` is used, the device will not output valid data.

Example: If the application desires to read the first byte of the Serial Number, the word address input would need to be 80h.

Note: The entire 128-bit value must be read from the starting address of the Serial Number block to guarantee a unique number. Reading the Serial Number from a location other than the first address of the block will not result in a unique Serial Number.

When the end of the Security Register is reached (32 bytes of data), the data Word Address will roll over to the beginning of Security Register starting with the most significant byte of the 128-bit Serial Number. The Serial Number Read operation or any read of the Security Register is terminated when the Master does not respond with an ACK and instead issues a Stop condition.

Figure 8-1. Serial Number Read



Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, “Ordering Code Detail”).

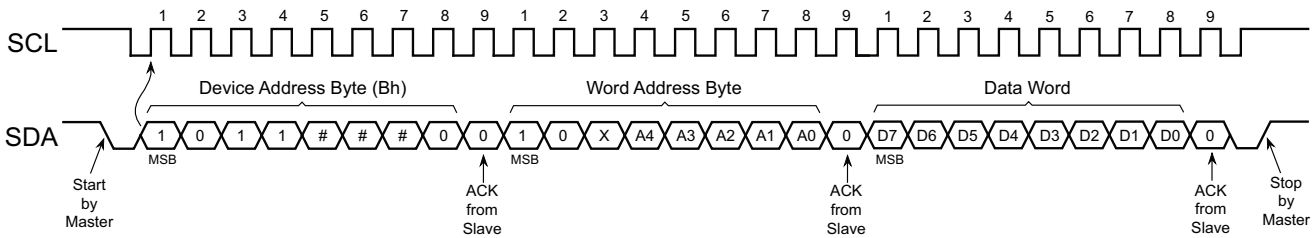
8.3 Write Operations in the Security Register

The Security Register supports Byte Writes, Page Writes, and Partial Page Writes in the upper 16 bytes of the region. Page Writes and Partial Page Writes in the Security Register have the same page boundary restrictions and behavior as they do in the EEPROM region (see Section 5.2 “Page Write” on page 13).

Writing in the Security Register requires beginning the Device Address byte with `1011b` (Bh), matching the Hardware Address bits (A_2, A_1, A_0) to the corresponding value determined by the ordering code (see Section 11.1), and sending a Logic 0 in the Read/Write Select bit. The device will ACK this sequence.

Following the Device Address Byte, bits A7 and A6 of the Word Address byte must be set to `10b` regardless of the intended address being written. Refer to Table 4-2 and Table 4-3 on page 12 for detailed requirements on these bits. Figure 8-2 is included below as an example of a Byte Write operation in the Security Register.

Figure 8-2. Byte Write in the Security Register



Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1).

The user-programmable portion of the Security Register can be permanently inhibited from future writing with the Lock command. The status of the Lock state can be determined by sending a subset of the Lock command.

8.3.1 Lock Command

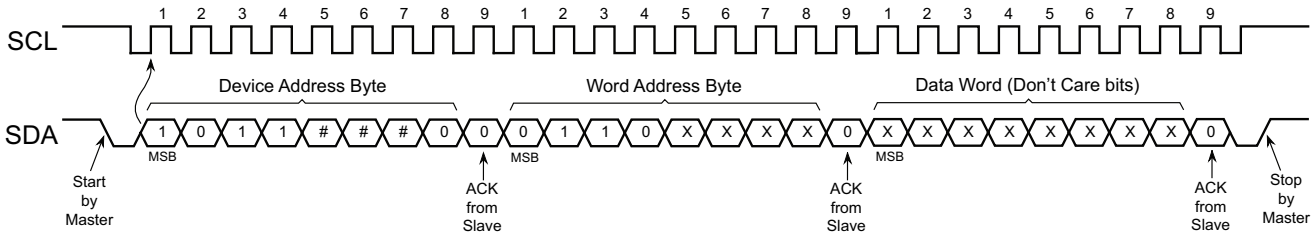
The Lock command is an irreversible sequence that will permanently prevent all future writing to the Security Register. Once the Lock command has been executed, the Security Register becomes read-only.

Warning: Once the Security Register has been locked, *it cannot be unlocked.*

The Lock command protocol emulates a Byte Write operation to the Security Register. However, the A7 through A4 bits of the Word Address must be set to `0110b` (6h). The remaining bits of the Word Address and the Data Byte are don't care bits. Even though these bits are don't care values, they must be transmitted to the device. An ACK response to the Word Address and data word byte indicates the Security Register is not currently locked. A NACK response indicates the AT24CSW01x/02x is already locked. Please refer to Section 8.3.2 for details about determining the Lock status of the AT24CSW01x/02x.

The sequence completes with a Stop condition being sent to the device, which initiates a self-timed internal write cycle. The Lock operation will conclude upon completion of that write cycle, subsequently making the Security Register permanently read-only. Read operations are always allowed to the device.

Figure 8-3. Lock Command

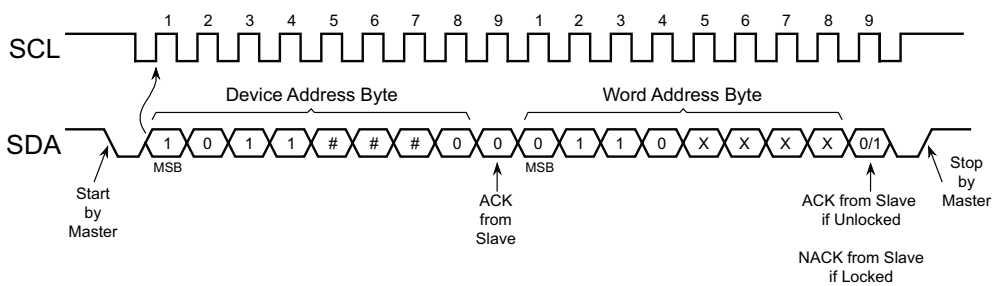


Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1, "Ordering Code Detail").

8.3.2 Determining the Lock State of the Security Register

The Lock state of the device can be determined by sending a subset of the Lock command to the device. Only the Device Address byte and Word Address byte need to be transmitted to the device to determine the Lock state. An ACK response to the Word Address byte indicates the Lock has not been set while a NACK response indicates the Lock has been set. If the Lock has already been set, it cannot be undone. The abbreviated Lock sequence is completed by the Master sending a Stop condition to the device.

Figure 8-4. Determining the Security Register Lock State



Note: # indicates the Hardware Address value which is managed by the ordering code of the device (see Section 11.1).

9. Device Default Condition from Atmel

The AT24CSW01x/02x is delivered with the EEPROM array set to Logic 1 resulting in FFh data throughout the Memory Array.

The Security Register contains a pre-programmed 128-bit Serial Number in the lower 16 bytes. The upper 16 bytes of this register is set to Logic 1 resulting in FFh data.

The device is delivered with the Security Register Lock function not enabled (see Section 8.3.1, “Lock Command”), and the Write Protection Register set to 00h.

10. Electrical Specifications

10.1 Absolute Maximum Ratings

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Supply Voltage with respect to ground	-0.5V to +4.10V
Voltage on any pin with respect to ground	-0.6V to V_{CC} + 0.5V
DC Output Current	5.0mA

Functional operation at the “Absolute Maximum Ratings” or any other conditions beyond those indicated in Section 10.2 “DC and AC Operating Range”is not implied or guaranteed. Stresses beyond those listed under “Absolute Maximum Ratings” and/or exposure to the “Absolute Maximum Ratings” for extended periods may affect device reliability and cause permanent damage to the device.

The voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot pulses that the device may be subjected to during the course of normal operation and does not imply or guarantee functional device operation at these levels for any extended period of time.

10.2 DC and AC Operating Range

Table 10-1. DC and AC Operating Range

		AT24CSW01x/02x Series
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low Voltage Grade	1.7V to 3.6V

10.3 DC Characteristics

Table 10-2. DC Characteristics

Parameters are applicable over the operating range in Section 10.2, unless otherwise noted.

Symbol	Parameter	Test Condition		Min	Typical(1)	Max	Units
V_{CC}	Supply Voltage			1.7		3.6	V
I_{CC1}	Supply Current, Read	V_{CC} = 1.8V(2)	Read at 400kHz	—	0.08	0.3	mA
		V_{CC} = 3.6V	Read at 1MHz	—	0.15	0.5	
I_{CC2}	Supply Current, Write	V_{CC} = 3.6V	Write at 1MHz	—	0.20	1.0	
I_{SB}	Standby Current	V_{CC} = 1.8V(2)	V_{IN} = V_{CC} or V_{SS}	—	0.08	0.4	µA
		V_{CC} = 3.6V		—	0.10	0.8	
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		—	0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		—	0.05	3.0	
V_{IL}	Input Low Level(2)			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level(2)			V_{CC} x 0.7		V_{CC} + 0.5	
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15mA	—		0.2	V
V_{OL2}		V_{CC} = 3.0V	I_{OL} = 2.1mA	—		0.4	

Notes: 1. Typical values characterized at T_A = +25°C unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.

10.4 AC Characteristics

Table 10-3. AC Characteristics

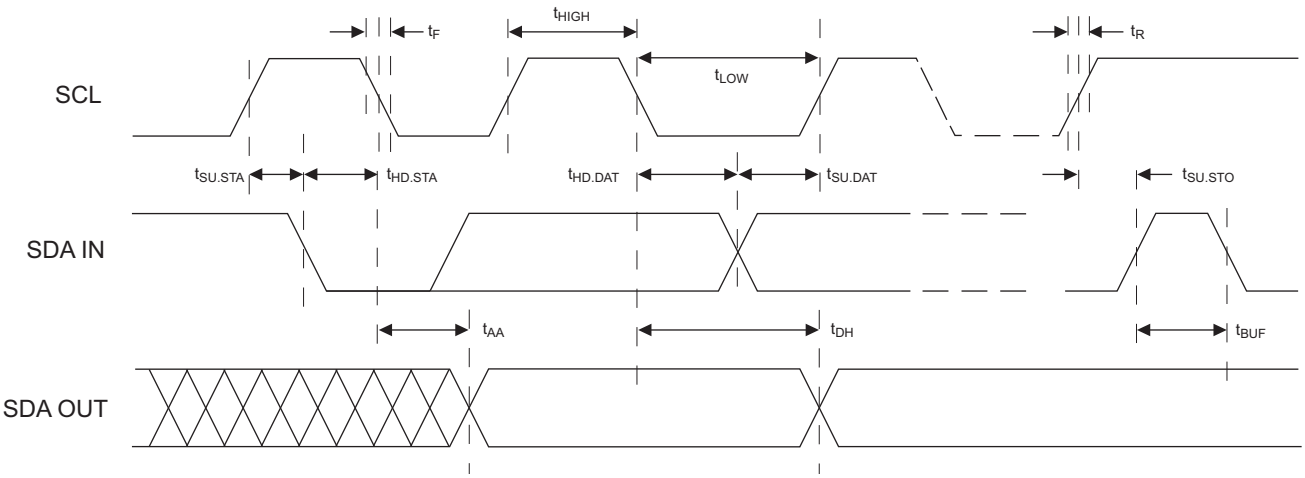
Parameters are applicable over operating range in Section 10.2 unless otherwise noted. Test conditions shown in Note 2.

Symbol	Parameter	Standard Mode V_{CC} = 1.7V to 3.6V		Fast Mode V_{CC} = 1.7V to 3.6V		Fast Mode Plus V_{CC} = 1.7V to 3.6V		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	4,700		1,300		500		ns
t_{HIGH}	Clock Pulse Width High	4,000		600		400		ns
t_I	Input Filter Spike Rejection (SCL, SDA)(1)		100		100		100	ns
t_{AA}	Clock Low to Data Out Valid		4,500		900		450	ns
t_{BUF}	Bus Free Time between Stop and Start(1)	4,700		1,300		500		ns
$t_{HD.STA}$	Start Hold Time	4,000		600		250		ns
$t_{SU.STA}$	Start Set-up Time	4,700		600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	200		100		100		ns
t_R	Inputs Rise Time(1)		1,000		300		100	ns
t_F	Inputs Fall Time(1)		300		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	4,700		600		250		ns
t_{DH}	Data Out Hold Time	100		50		50		ns
t_{WR}	Write Cycle Time		5		5		5	ms

Notes: 1. These parameters are determined through product characterization and are not tested 100% in production.

2. AC measurement conditions:
   - C_L : 100pF
   - R_{PUP} (bus line pull-up resistor to V_{CC}): 1.3kΩ (1000kHz), 4kΩ (400kHz), 10kΩ (100kHz)
   - Input pulse voltages: 0.3 x V_{CC} to 0.7 x V_{CC}
   - Input rise and fall times: ≤ 50ns
   - Input and output timing reference voltages: 0.5 x V_{CC}

Figure 10-1. Bus Timing



10.5 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT24CSW01x/02x should monotonically rise from GND to the minimum V_{CC} level as specified in Section 10.2 with a slew rate no faster than 0.1V/µs.

10.5.1 Device Reset

To prevent write operations or other spurious events from happening during a power-up sequence, the AT24CSW01x/02x includes a Power-On-Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of reset and into standby mode.

The system designer must ensure that instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than the minimum V_{CC} level. Additionally, once the V_{CC} is greater than the minimum V_{CC} level, the bus Master must wait at least t_{PUP} before sending the first command to the device. See Table 10-4 for the values associated with these power-up parameters.

Table 10-4. Power-up Conditions

Symbol	Parameter	Min	Max	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands.	100	—	µs
V_{POR}	Power-On-Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles.	1	—	ms

If an event occurs in the system where the V_{CC} level supplied to the AT24CSW01x/02x drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time, and then performing a new power-up sequence in compliance with the requirements defined in this section.

10.6 Pin Capacitance

Table 10-5. Pin Capacitance(1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = 3.6V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized but is not 100% tested in production.

10.7 EEPROM Cell Performance Characteristics

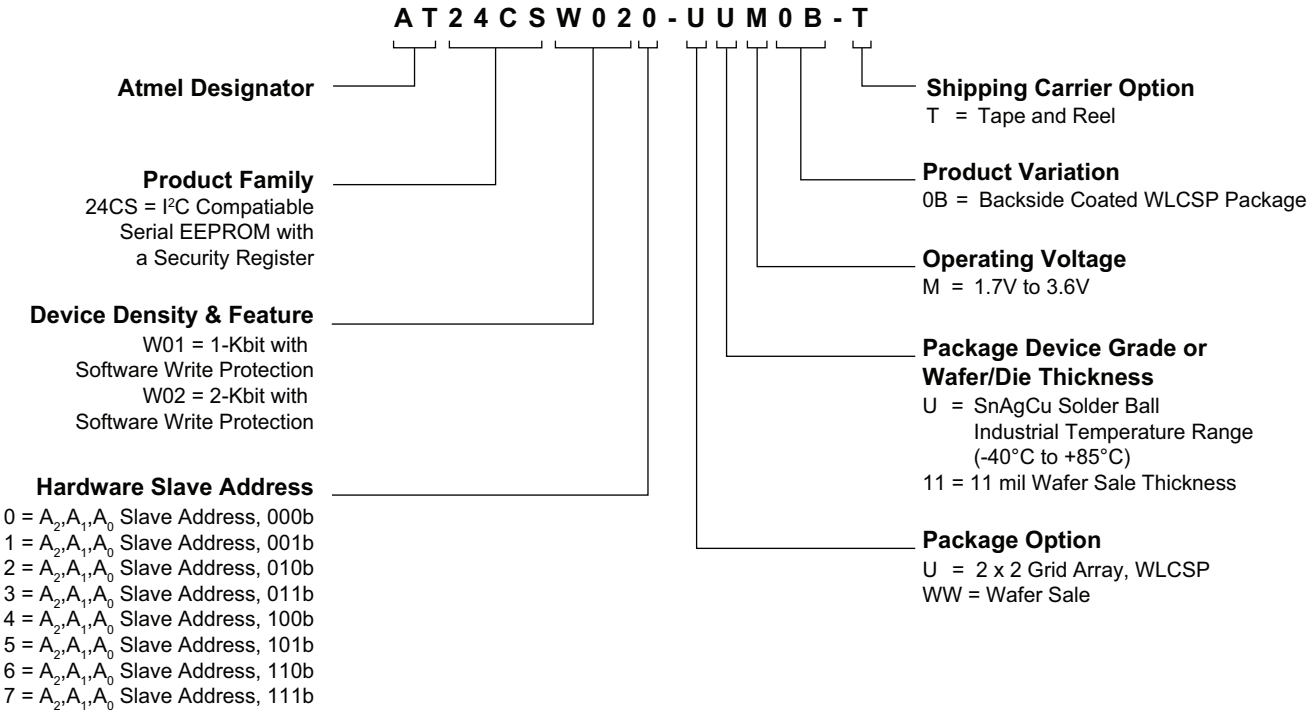
Table 10-6. EEPROM Cell Performance Characteristics

Operation or Parameter	Test Condition	Min	Max	Units
Write Endurance(1)	T_A = 25°C, V_{CC}(min) < V_{CC} < V_{CC}(max) Byte or Page Write Mode	1,000,000	—	Write Cycles
Data Retention(2)	T_A = 55°C, V_{CC}(min) < V_{CC} < V_{CC}(max)	100	—	Years

Notes: 1. Write Endurance performance is determined through characterization and the qualification process.
2. The data retention capability is determined by qualification and checked on each device during production.

11. Ordering Information

11.1 Ordering Code Detail



11.2 Ordering Information

Additional package types that are not listed below can be made available. Please contact Atmel for more details.

Atmel Ordering Code[1]	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT24CSW010-UUM0B-T	SnAgCu (Lead-free/Halogen-free)	4U-13	Tape and Reel	5,000 per Reel	Industrial Temperature (-40°C to 85°C)
AT24CSW011-UUM0B-T					
AT24CSW012-UUM0B-T					
AT24CSW013-UUM0B-T					
AT24CSW014-UUM0B-T					
AT24CSW015-UUM0B-T					
AT24CSW016-UUM0B-T					
AT24CSW017-UUM0B-T					
AT24CSW020-UUM0B-T	SnAgCu (Lead-free/Halogen-free)	4U-13	Tape and Reel	5,000 per Reel	Industrial Temperature (-40°C to 85°C)
AT24CSW021-UUM0B-T					
AT24CSW022-UUM0B-T					
AT24CSW023-UUM0B-T					
AT24CSW024-UUM0B-T					
AT24CSW025-UUM0B-T					
AT24CSW026-UUM0B-T					
AT24CSW027-UUM0B-T					

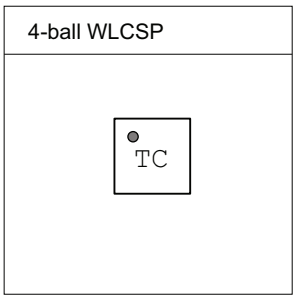
Notes: 1. WLCSP Package:

- This device includes a backside coating to increase product robustness.
- **CAUTION:** Exposure to ultraviolet (UV) light can degrade the data stored in the EEPROM cells. Therefore, customers who use a WLCSP product must ensure that exposure to ultraviolet light does not occur.

Package Type	
4U-13	4-ball, 2 x 2 Grid Array, Ultra-thin Wafer Level Chip Scale Package (WLCSP)

11.3 Part Marking

AT24CSW01 and AT24CSW02 Series: Package Marking Information



Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

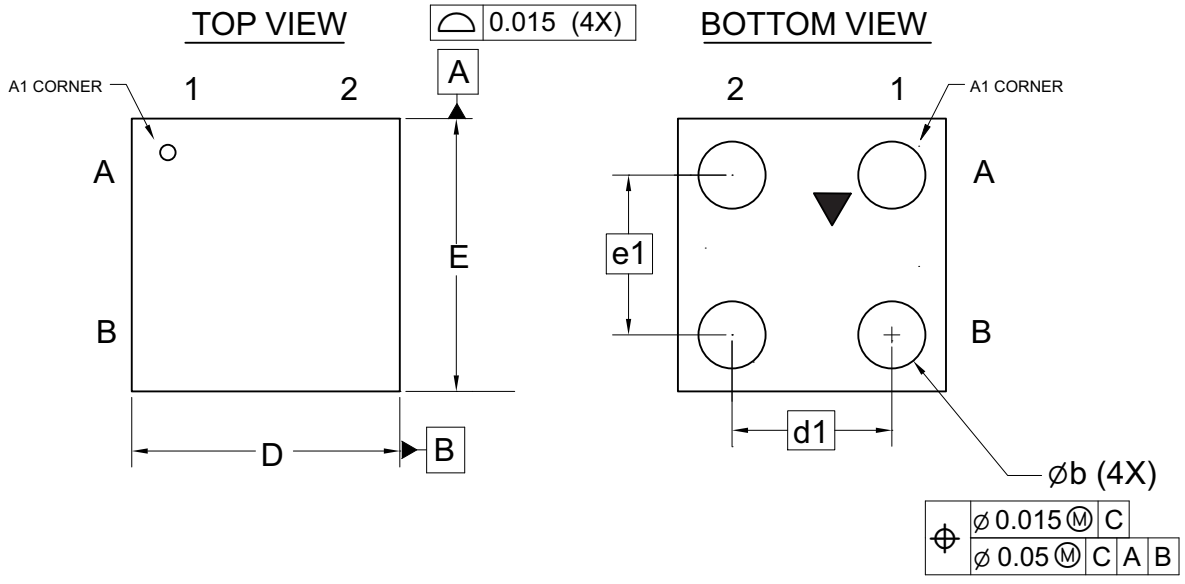
Catalog Number Truncation			
AT24CSW01x,		Truncation Code ###: N1A	
AT24CSW02x		Truncation Code ###: N2A	
Date Codes			**Voltages**
Y = Year		M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014	8: 2018	A: January	02: Week 2	M: 1.7V min
5: 2015	9: 2019	B: February	04: Week 4	
6: 2016	0: 2020	...	...	
7: 2017	1: 2021	L: December	52: Week 52	
Country of Assembly		**Lot Number**	**Grade/Lead Finish Material**
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number	U: Industrial/Matte Tin
Trace Code			**Atmel Truncation**
TC = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

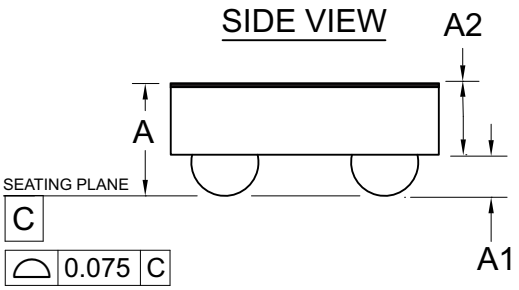
12/4/15

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **24CSW01_24CSW02SM**, AT24CSW01-02 Series Package Marking Information	**DRAWING NO.** 24CSW01_02SM	**REV.** A

12. Packaging Information

12.1 4U-13 — 4-ball WLCSP





PIN ASSIGNMENT MATRIX

	1	2
A	V_{CC}	V_{SS}
B	SCL	SDA

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.260	0.295	0.330	
A1	—	0.070	—	
A2	—	0.225	—	3
D	Contact Atmel for Details			
d1	0.400 BSC			
E	Contact Atmel for Details			
e1	0.400 BSC			
b	—	0.162	—	

Note: 1. Dimensions are NOT to scale.
2. Solder ball composition is 95.5Sn-4.0Ag-0.5Cu.
3. Product offered with Back Side Coating (BSC)

10/1/15

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 4U-13, 4-ball 2x2 Array, 0.40mm Pitch Wafer Level Chip Scale Package (WLCSP) with BSC	GPC GUJ	DRAWING NO. 4U-13	REV. A

13. Revision History

Doc. No.	Date	Comments
8982B	01/2017	Updated from Preliminary to Complete status Updated Power On Requirements and Reset Behavior section
8982A	07/2016	Initial document release, Preliminary status.

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