PIC24HJXXXGPXXX

PIC24H Engineering Samples Rev. A0/A1 Silicon Errata

PIC24HJXXXGPXXX, (Rev. A0/A1) Silicon Errata

The PIC24H Engineering Samples (Rev. A0/A1) you received were found to conform to the specifications and functionality described in the following documents:

- DS70175 – "*PIC24H Family Data Sheet*"
- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"
- DS70046 – "*dsPIC30F Family Reference Manual*"

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- PIC24HJ128GP506-PT ES
- PIC24HJ256GP206-PT ES
- PIC24HJ256GP610-PF ES
- PIC24HJ256GP610-PT ES

PIC24H Rev. A0/A1 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 with MPLAB IDE v7.31.01 or later. The output window will show either:

1. A successful connection to the device specified in *Configure>Select Device*
2. Warning message `ICD Warn0020: Invalid target device id`. If this message is received, consult the *"dsPIC33F Flash Programming Specification"* (DS70152) to verify the device ID. This document contains device IDs for both the dsPIC33F and PIC24H devices. This device mismatch will be fixed in future revisions of MPLAB IDE.

The errata described in this section will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. SPI with 1:1 Prescaler

   The SPI modules do not function correctly when the SPI clock prescale ratio is set to 1:1.

2. SPI Master Reception for Bit Rates above 8 Mbps

   SPI Master reception does not function correctly at bit rates higher than 8 Mbps, if the data is sampled at the middle of the serial clock period.

3. ADC with Sample/Hold CH3

   Sample/Hold amplifier CH3 does not function correctly for the Analog-to-Digital Converter modules.

4. LATC and LATD Reads

   The LATC and LATD register reads do not function.

5. DMA Single-Shot Mode

   The Direct Memory Access Single-Shot mode does not function correctly.

6. Windowed Watchdog Timer

   When the Windowed WDT option is enabled and the WDT is disabled, a WDT time out will occur.

7. Timer3 as A/D Conversion Trigger Source

   Timer2 and Timer3, when configured as a single 32-bit timer, may not initiate an A/D conversion if the PR3 register is set to '0' and Timer3 is selected as the A/D conversion trigger source.

8. UART Auto-Baud

   The UART FIFO will be loaded with incorrect data if the UxBRG register is not initialized to a specific value.

9. Doze Mode

   When Doze mode is enabled, any writes to a peripheral SFR can cause other updates to that register to cease to function for the duration of the current CPU clock cycle.

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10. 12-bit ADC Module

    For this revision of silicon, the 12-bit ADC module INL and DNL, conversion speed and signal acquisition time parameters are not within the published data sheet specifications.

11. 10-bit ADC Module

    For this revision of silicon, the 10-bit ADC module INL, DNL and signal acquisition time parameters are not within the published data sheet specifications.

12. DMA Module: Interaction with `EXCH` Instruction

    The `EXCH` instruction does not execute correctly when one of the operands contains a value equal to the address of the DMAC SFRs.

13. `DISI` Instruction

    The `DISI` instruction will not disable interrupts if a `DISI` instruction is executed in the same instruction cycle that the `DISI` counter decrements to zero.

14. JTAG Programming

    JTAG programming will not work in silicon revision A0/A1.

15. Internal FRC Oscillator

    The internal FRC oscillator is not calibrated in silicon revision A0/A1.

16. ECAN™ Loopback Mode

    The ECAN module (ECAN1 or ECAN2) does not function correctly in Loopback mode.

17. Clock Switch From Fail-Safe Clock Source

    Once a clock fail interrupt has occurred, the clock source cannot be switched from the fail-safe clock source.

18. I^{2}C™ Module

    The I^{2}C module does not wake-up from Sleep when it detects bus activity.

The following sections will describe the errata and work around to these errata, where they may apply.

1. Module: SPI with 1:1 Prescaler

The SPI1 and SPI2 modules do not generate any serial clock signals and, therefore, do not function correctly for the following values of the PPRE<1:0> (SPIxCON1<1:0>) and the SPRE<2:0> (SPIxCON1<4:2>) bits:

- PPRE = 11, SPRE = 111

Work around

Users may set up the SPI module with any prescale ratio other than 1:1.

2. Module: SPI Master Reception for Bit Rates above 8 Mbps

Master mode receptions using the SPI1 and SPI2 module do not function correctly for bit rates above 8 Mbps if the Master has the SMP bit (SPIxCON1<9>) cleared (Master samples data at the middle of the serial clock period).

In this case, the data transmitted by the Slave is received shifted right by one bit by the Master. For example, if the data transmitted by the Slave was 0xAAAA, the data received by the Master would be 0x5555 (0xAAAA shifted right by one bit).

Work around

Users may set up the SPI module so that the bit rate is 8 Mbps or lower.

Alternatively, the bit rate can be configured higher than 8 Mbps, but the SMP bit (SPIxCON1<9>) of the SPI Master must be set (Master samples data at the end of the serial clock period).

3. Module: ADC with Sample/Hold CH3

The Sample/Hold amplifier CH3 does not function correctly when used with the Analog-to-Digital Converter (ADC) modules. The corresponding conversion result is always read as 0x0000.

Work around

Do not use the Sample/Hold amplifier CH3 with the ADC1 or ADC2 module. You may use CH0, CH1 and CH2.

4. Module: LATC and LATD Reads

The LATC and LATD register reads do not function. Performing a read or read-modify-write operation on the LATC register or the LATD register will not function.

Do not perform read or read-modify-write operations on the LATC and LATD registers. Inspect the disassembly listing of any user application software that may be accessing the LATC or LATD register, to ensure that read or read-modify-write operations are not being performed on these registers.

To verify the contents of the LATC register, perform the following steps:

- Write to LATC
- Make a PORTC pin an output
- Read the PORTC register

The same steps can be performed to verify the contents of the LATD register.

Note: The Port pin state, and therefore the read value, depends on the load attached to the Port pin.

5. Module: DMA Single-Shot Mode

The DMA Single-Shot mode does not function correctly for more than one block transfer. After one block transfer, the DMA channel becomes unusable until a device reset occurs.

Work around

If more than one DMA data block transfers are required during the entire program execution, the user application may set up the required DMA channel to operate in Continuous mode, and disable the DMA channel every time the corresponding DMA interrupt has occurred.

However, if only one DMA data block transfer is required for a particular DMA channel during the entire program execution, the Single-Shot mode may be used.

6. Module: Watchdog Timer

When the WDT is disabled and the WDT Window is enabled, a WDT time out will occur. This will cause the device to reset unexpectedly. The WDT is disabled by clearing the FWDTEN bit (FWDT<7>). The WDT Window feature is enabled by clearing the WINDIS bit (FWDT<6>).

Work around

In order to prevent an unexpected WDT time out when the WDT is disabled, disable the WDT Window feature by setting the WINDIS bit (FWDT<6>).

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7. Module: ADC with Timer as Conversion Trigger Source

The ADC module can be configured so that Timer3 ends ADC sampling and starts the conversion (ADCON<7:5> = 010). PR3, the Timer3 period register, is loaded with a value that is compared to TMR3. In the ADC mode described, when TMR3 is equal to PR3, an A/D conversion is initiated.

Timer3 can also initiate an A/D conversion when Timer2 and Timer3 are configured as a single 32-bit timer. However, when Timer2 and Timer3 are configured as a single 32-bit timer, an A/D conversion may not be initiated if the PR3 register is set to '0'.

Work around

When Timer3 is selected as the trigger for initiating an A/D conversion (i.e. ADCON<7:5> = 010), make sure that PR3 is non-zero.

8. Module: UART Auto-Baud

When auto-baud is enabled (UxMODE<5> is set), the UART FIFO will be loaded with incorrect data unless the UxBRG register is initialized to 0xFFFF.

Work around

Initialize the UxBRG register to 0xFFFF anytime auto-baud is enabled.

9. Module: Oscillator: Doze Mode

Enabling Doze mode slows down the CPU but allows peripherals to run at full speed. When the CPU clock is slowed down by enabling Doze mode (CLKDIV<11> = 1), any writes to a peripheral SFR can cause other updates to that register to cease to function for the duration of the current CPU clock cycle. This is only an issue if the CPU attempts to write to the same register as a peripheral while in Doze mode.

For instance, if the ADC module is active and Doze mode is enabled, the main program should avoid writing to ADCCONx registers because these registers are being used by the ADC module. If the CPU does make writes before the ADC module does, then any attempts by the ADC module to write to these registers will fail.

Work around

In Doze mode, avoid writing code that will modify SFRs which may be written to by enabled peripherals.

10. Module: 12-bit ADC

1. When the ADC module is configured for 12-bit operation, the ADC INL is >±2 LSBs and DNL is >±1 LSB.
2. The conversion speed is limited to 400 Ksps and requires a minimum signal acquisition time of 266 nS.

Work around

Implement the ADC module as either a 10 or 11-bit A/D Converter.

1. When used as a 10-bit ADC, the INL is <±2 LSBs, and DNL is <±1 LSB with no missing codes.
2. When used as an 11-bit ADC, the INL is <±2 LSBs and DNL is ±1 LSB with missing codes at each 2^7 power boundary. ADC monotonicity is still realized if the missing codes are ignored.

Future versions of the silicon will support full 12-bit operation with <±2 LSBs INL and <±1 LSB DNL, a 500 Ksps conversion rate and a 133 nS signal acquisition time.

11. Module: 10-bit ADC

The ADC module INL is >±2 LSBs and DNL is >±1 LSB.

Work around

None. Future versions of the silicon will support <±2 LSBs INL and <±1 LSB DNL specifications, and a 70 nS signal acquisition time.

12. Module: DMA Module: Interaction with `EXCH` Instruction

The `EXCH` instruction does not execute correctly when either of the two operands is numerically equal to the address of any of the DMAC SFRs for this revision of silicon.

Work around

If writing source code in assembly, the recommended fix is to replace:

```
        EXCH Wsource, Wdestination
```
with:
```
        PUSH Wdestination
        MOV Wsource, Wdestination
        POP Wsource
```

If using the MPLAB C30 C compiler, check the disassembly listing (*View>Disassembly Listing*) for the `EXCH` instruction. If used, make sure the operands are not equivalent to the DMA SFRs' addresses.

13. Module: `DISI` Instruction

When a user executes a `DISI` #7, for example, this will disable interrupts for 7 + 1 cycles (7 + the `DISI` instruction itself). In this case, the `DISI` instruction uses a counter which counts down from 7 to 0. The counter is loaded with 7 at the end of the `DISI` instruction.

If the user code executes another `DISI` on the instruction cycle where the `DISI` counter has become zero, the new `DISI` count is loaded, but the `DISI` state machine does not properly re-engage and continue to disable interrupts. At this point, all interrupts are enabled. The next time the user code executes a `DISI` instruction, the feature will act normally and block interrupts.

In summary, it is only when a `DISI` execution is coincident with the current `DISI` count = 0, that the issue occurs. Executing a `DISI` instruction before the `DISI` counter reaches zero will not produce this error. In this case, the `DISI` counter is loaded with the new value, and interrupts remain disabled until the counter becomes zero.

Work around

When executing multiple `DISI` instructions within the source code, make sure that subsequent `DISI` instructions have at least one instruction cycle between the time that the `DISI` counter decrements to zero and the next `DISI` instruction. Alternatively, make sure that subsequent `DISI` instructions are called before the `DISI` counter decrements to zero.

14. Module: JTAG Programming

JTAG programming does not work in silicon revision A0/A1.

Work around

None.

15. Module: Internal FRC Oscillator

The internal FRC oscillator is not calibrated on silicon revision A0/A1.

Work around

The user can calibrate the internal oscillator manually by modifying the OSCTUN bits. This is done by using a waveform generator or other external source to generate a square wave of known frequency on one of the input capture pins. Configure the corresponding Input Capture module to measure the square wave period. Calculate the value that the input capture module should generate based on a nominal internal FRC oscillator frequency of 7.37 MHz. Adjust the OSCTUN bits until the measured input capture value matches the calculated value.

16. Module: ECAN Loopback Mode

The ECAN module (ECAN1 or ECAN2) does not function correctly in Loopback mode.

Work around

Do not use Loopback mode.

17. Module: Oscillator Configuration Block

If the fail-safe clock monitoring function is enabled, during a failure of the external oscillator, the device will automatically switch to the internal FRC oscillator. A clock failure trap event is also generated. In revision A0/A1 parts, once this interrupt occurs, the clock source cannot be switched from the internal FRC oscillator.

Work around

The user must issue a Reset before attempting to change clock sources after a clock fail event.

18. Module: I^{2}C

The I^{2}C module does not wake-up from Sleep when it detects bus activity.

Work around

None.

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APPENDIX A: REVISION HISTORY

Revision A (2/2006)

- First release of the document.

Revision B (5/2006)

- Added silicon issues 6 (Windowed Watchdog Timer, 7 (Timer3 as A/D Conversion Trigger Source), 8 (UART Auto-Baud), 9 (Doze Mode), 10 (12-bit ADC), 11 (10-bit ADC), 12 (DMA Module: Interaction with EXCH Instruction), 13 (DISI Instruction), 14 (JTAG Programming), 15 (Internal FRC Oscillator), 16 (ECAN Loopback Mode), 17 (Clock Switch from Fail-Safe Clock Source) and 18 (I^2C Module).

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