

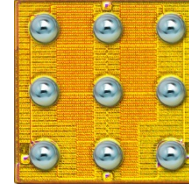
# EPC2110 – Dual Enhancement Mode Power Transistor Preliminary Specification Sheet



Status: Engineering

Features:

- $V_{DS}$ , 120V
- Dual FET, Common Source
- Maximum  $R_{DS(on)}$ , 60 m $\Omega$
- $I_D$ , 3.4 A
- Pulsed  $I_D$ , 20 A
- Pb-Free (RoHS Compliant), Halogen Free

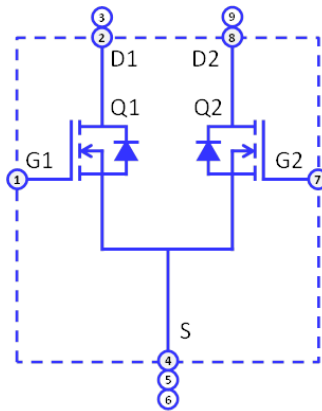


EPC2110 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 1.35 mm x 1.35 mm

Applications:

- Ultra High Frequency DC-DC Conversion
- Wireless Power Transfer
- Synchronous Rectification



MAXIMUM RATINGS

Parameter	Value
	Q1 Control FET / Q2 Sync FET
Maximum Drain – Source Voltage	120 V
Gate – Source Maximum Voltage Range	-4 V < $V_{GS}$ < 6 V
Continuous Drain Current, ( $T_A = 25\text{ }^\circ\text{C}$ , $R_{\theta JA} = 100\text{ }^\circ\text{C/W}$ )	3.4 A
Maximum Pulsed Drain Current, 25 $^\circ\text{C}$ , $T_{pulse} = 300\text{ }\mu\text{s}$	20 A
Optimum Temperature Range	-40 $^\circ\text{C}$ < $T_J$ < 150 $^\circ\text{C}$

STATIC CHARACTERISTICS

Parameter	Conditions	Value
		Q1 Control FET / Q2 Sync FET
Maximum Drain – Source Leakage	$V_{DS} = 96\text{ V}$ , $V_{GS} = 0\text{ V}$	0.25 mA
Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 4\text{ A}$	60 m $\Omega$
Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 4\text{ A}$	45 m $\Omega$
Gate – Source Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 0.7\text{ mA}$	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	1 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -4\text{ V}$	-0.25 mA

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated  
 Specifications are with Substrate shorted to Source

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## DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value Q1 Control FET /Q2 Sync FET
$C_{ISS}$ (Input Capacitance)	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	80 pF
$C_{OSS}$ (Output Capacitance)		50 pF
$C_{RSS}$ (Reverse Transfer Capacitance)		0.75 pF
$Q_G$ (Total Gate Charge)	$V_{DS} = 60\text{ V}, I_D = 4\text{ A}, V_{GS} = 5\text{ V}$	0.8 nC
$Q_{GS}$ (Gate to Source Charge)	$V_{DS} = 60\text{ V}, I_D = 4\text{ A}$	0.25 nC
$Q_{GD}$ (Gate to Drain Charge)		0.19 nC
$Q_{G(TH)}$ (Gate Charge at Threshold)		0.17 nC
$Q_{OSS}$ (Output Charge)	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	4.9 nC
$Q_{RR}$ (Source-Drain Recovery Charge)		0

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise stated

Specifications are with Substrate shorted to Source

## THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	28	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	81	$^\circ\text{C}/\text{W}$

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

See [http://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details

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## Preliminary Specification Sheet



Figure 1: Typical Output Characteristics at 25°C

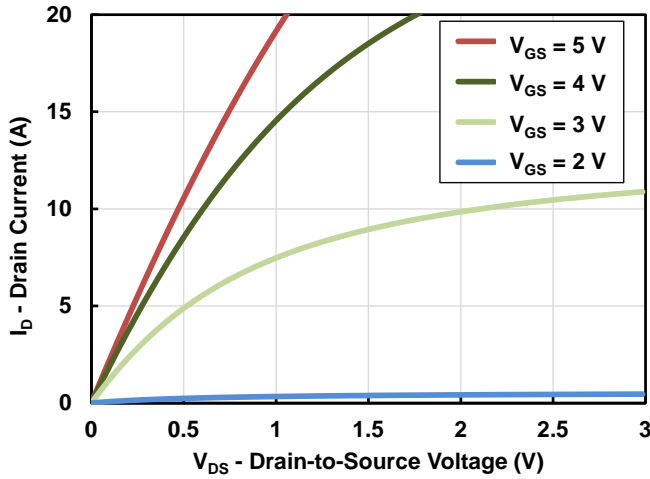


Figure 2: Transfer Characteristics

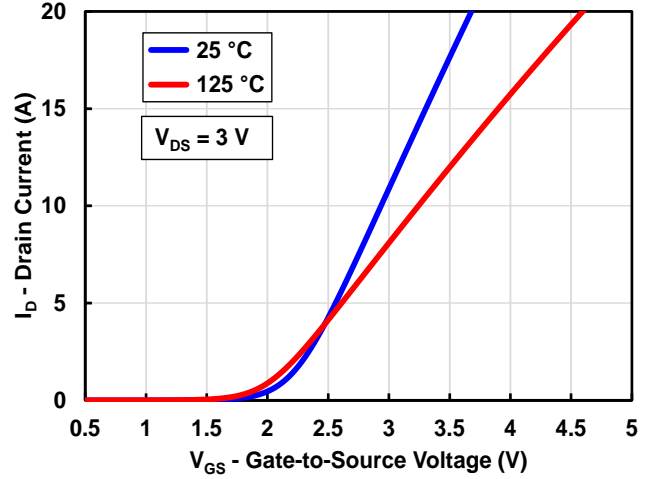


Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

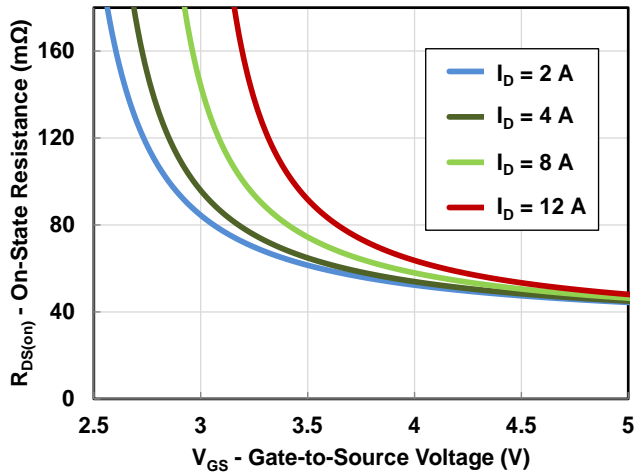


Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Temperatures

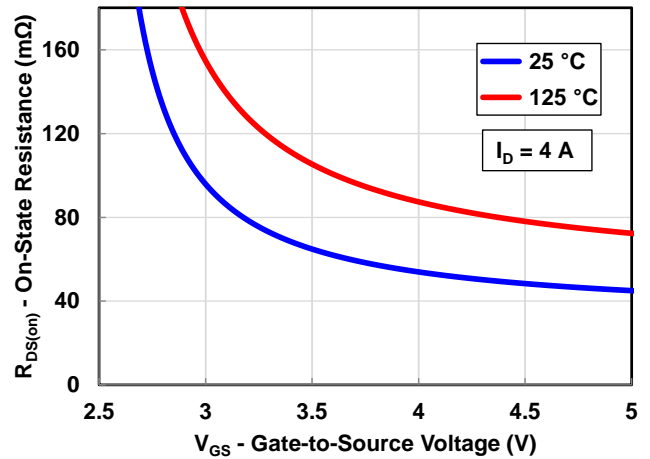


Figure 5a: Capacitance (Linear Scale)

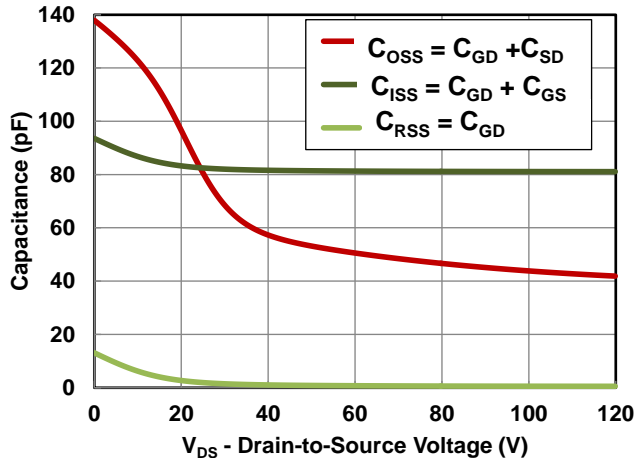
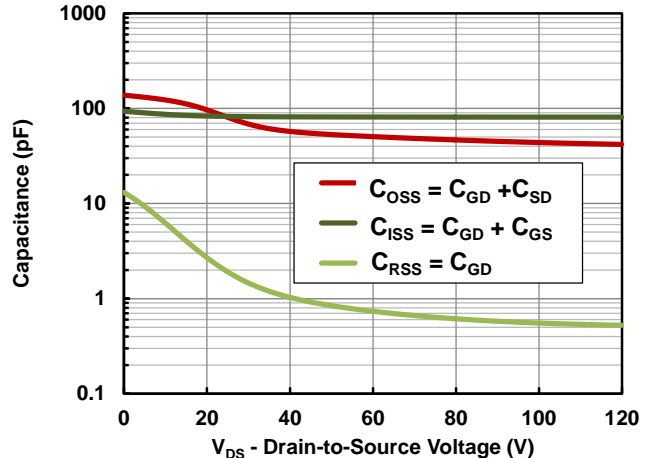


Figure 5b: Capacitance (Log Scale)



# EPC2110 – Dual Enhancement Mode Power Transistor

## Preliminary Specification Sheet



Figure 6: Gate Charge

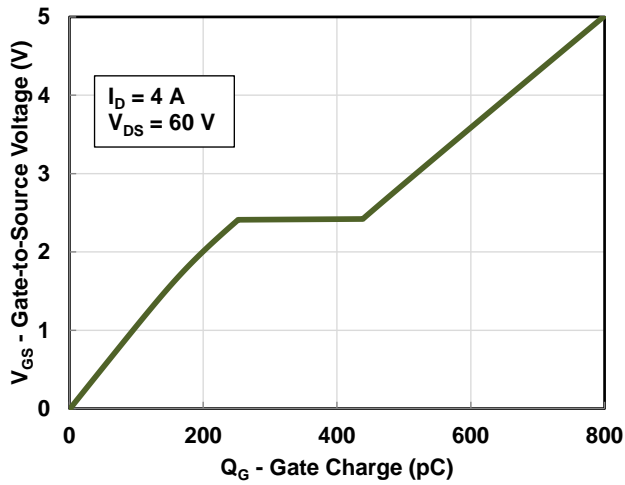


Figure 7: Reverse Drain-Source Characteristics

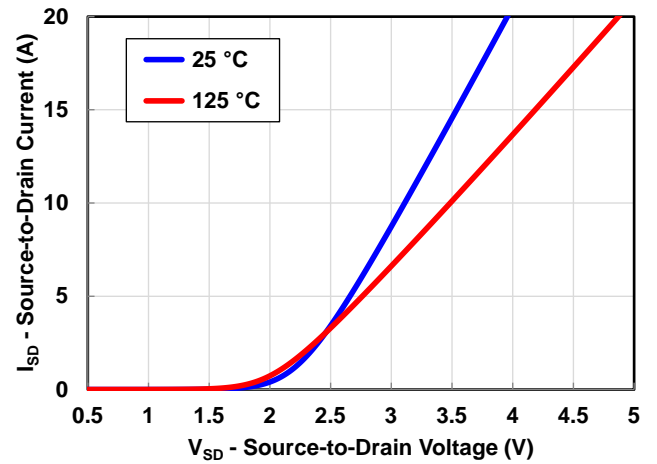


Figure 8: Normalized On Resistance vs. Temperature

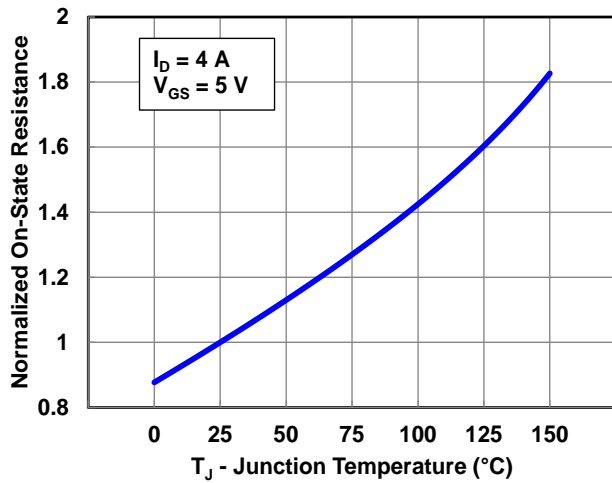


Figure 9: Normalized Threshold Voltage vs. Temperature

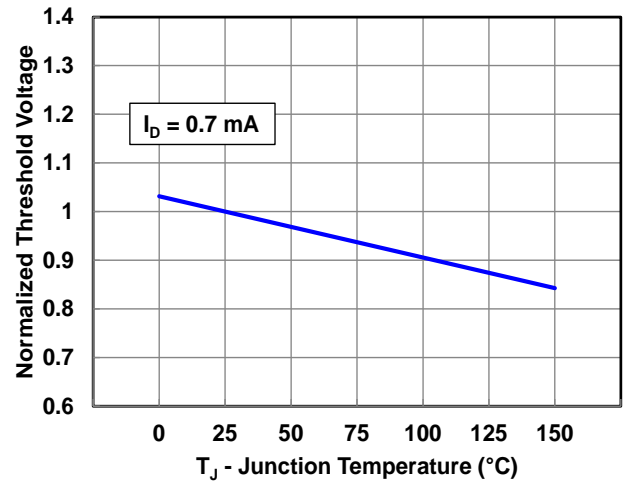
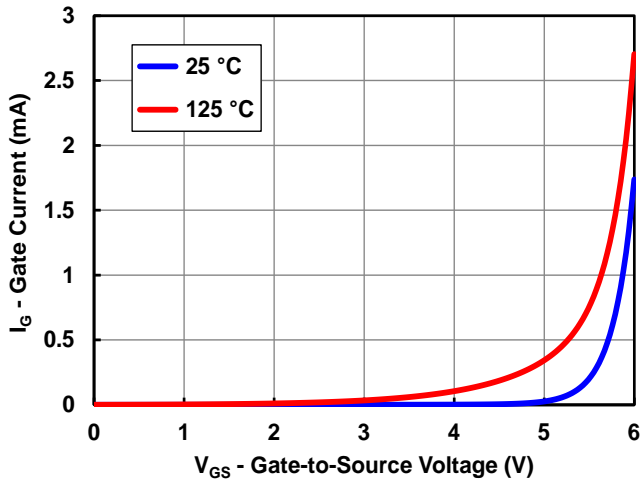


Figure 10: Gate-Source Characteristics



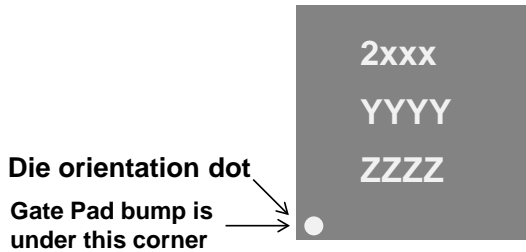
**Notes:**

1. All figures apply to both Q1 (Control FET) and Q2 (Sync FET)
2. All measurements were done with substrate shorted to source

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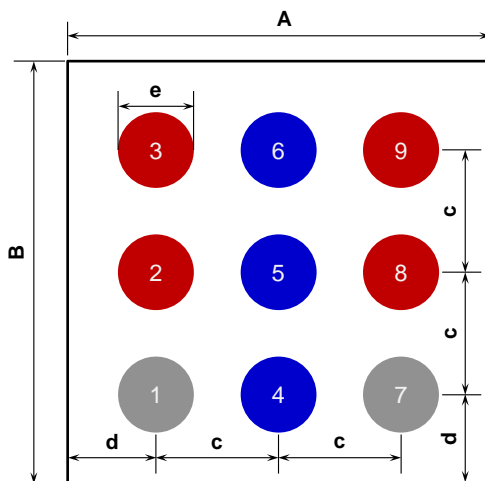
### DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2110ENGR	2XXX	YYYY	ZZZZ

### DIE OUTLINE

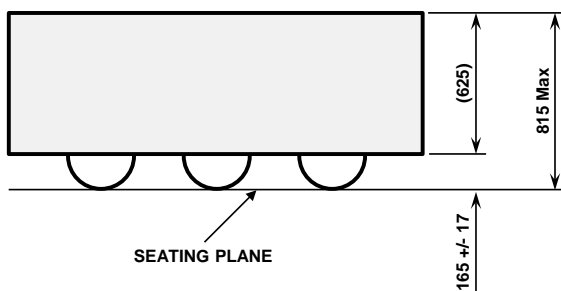
#### Solder Bar View



Pad 1 is Gate 1;  
 Pad 7 is Gate 2;  
**Pads 2, 3 are Drain 1;**  
**Pads 8, 9 are Drain 2;**  
**Pads 4, 5, 6 are Source**

DIM	MICROMETERS		
	MIN	Nominal	MAX
<b>A</b>	1320	1350	1380
<b>B</b>	1320	1350	1380
<b>c</b>	450	450	450
<b>d</b>	210	225	240
<b>e</b>	187	208	229

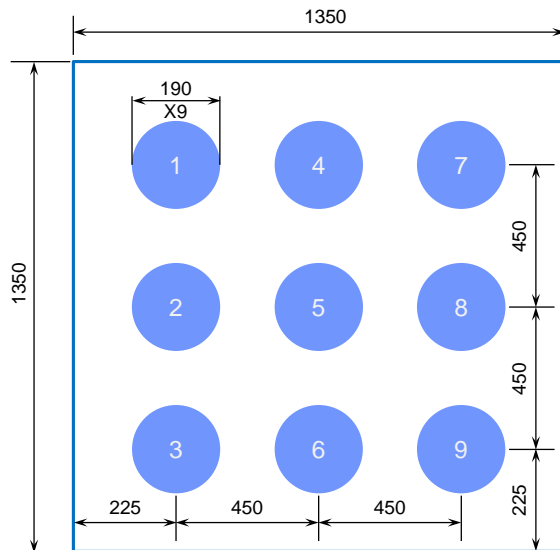
#### Side View



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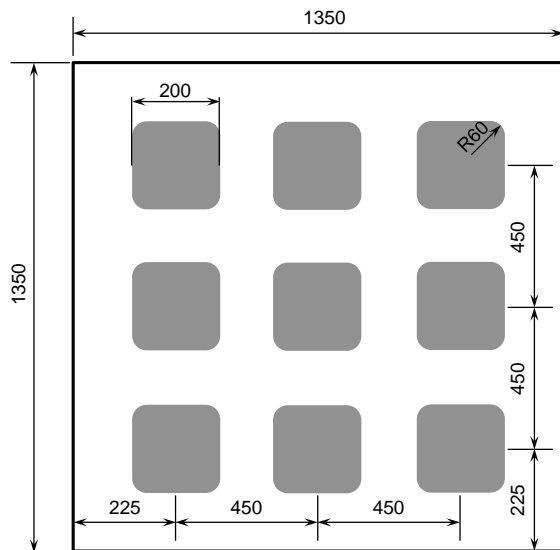
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### RECOMMENDED LAND PATTERN (Units in $\mu\text{m}$ )



**Pad 1 is Gate 1;**  
**Pad 7 is Gate 2;**  
**Pads 2, 3 are Drain 1;**  
**Pads 8, 9 are Drain 2;**  
**Pads 4, 5, 6 are Source**

### RECOMMENDED STENCIL DESIGN (Units in $\mu\text{m}$ )



Recommended stencil should be 4mil (100 $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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 U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

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