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# FDMS7578

## N-Channel Power Trench<sup>®</sup> MOSFET

25 V, 60 A, 5.8 mΩ

### Features

- Max  $r_{DS(on)}$  = 5.8 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 17\text{ A}$
- Max  $r_{DS(on)}$  = 8 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 14\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

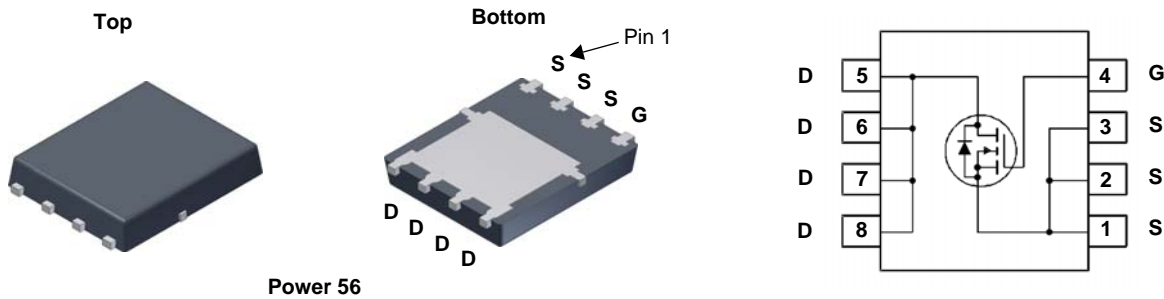


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### Applications

- Control MOSFET for Synchronous Buck Converters
- Notebook
- Server
- Telecomm
- High Efficiency DC-DC Switch Mode Power Supplies



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 20$	V
$I_D$	Drain Current -Continuous $T_C = 25\text{ °C}$	60	A
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	17	
	-Pulsed (Note 5)	90	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	40	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	33	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7578	FDMS7578	Power 56	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		20		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 17\text{ A}$		4.6	5.8	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 14\text{ A}$		6.3	8	
		$V_{GS} = 10\text{ V}$ , $I_D = 17\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		6.7	8.5	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 17\text{ A}$		77		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1221	1625	pF
$C_{oss}$	Output Capacitance			371	495	pF
$C_{riss}$	Reverse Transfer Capacitance			54	85	pF
$R_g$	Gate Resistance			1.2	2.4	$\Omega$

**Switching Characteristics**

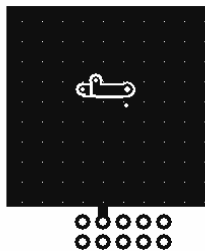
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}$ , $I_D = 17\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		8	17	ns
$t_r$	Rise Time			2.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			20	33	ns
$t_f$	Fall Time			2.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		18	25
	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 13\text{ V}$ $I_D = 17\text{ A}$	8	11	nC
$Q_{gs}$	Total Gate Charge			3.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.7		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.72	1.1	V
		$V_{GS} = 0\text{ V}$ , $I_S = 17\text{ A}$ (Note 2)		0.83	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		20	32	ns
$Q_{rr}$	Reverse Recovery Charge			6	12	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 17\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$		19	34	ns
$Q_{rr}$	Reverse Recovery Charge			13	24	nC

## NOTES:

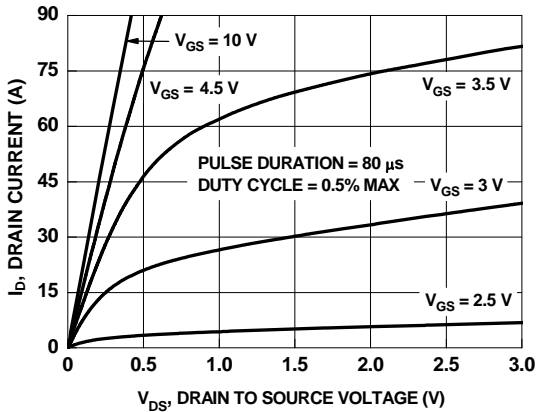
- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.


 a.  $50\text{ }^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper

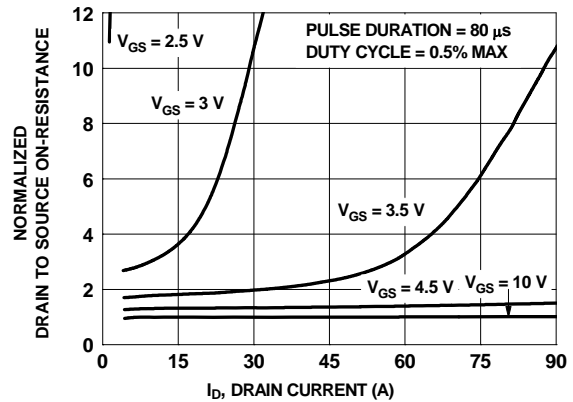
 b.  $125\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0 %.
- $E_{AS}$  of 40 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 14\text{ A}$ .
- As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

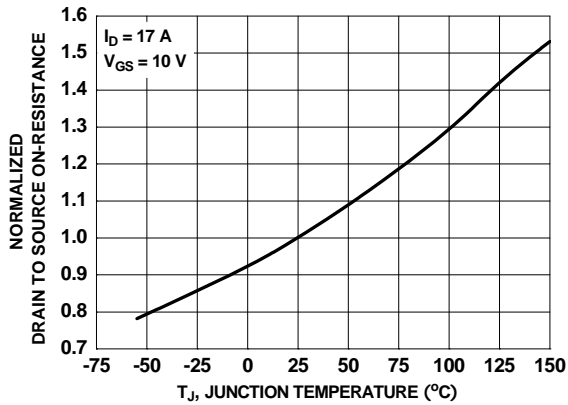
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



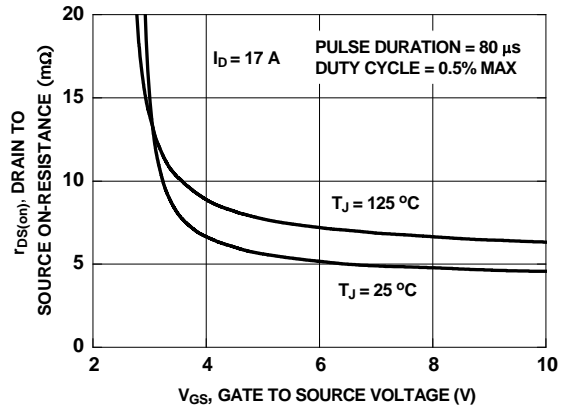
**Figure 1. On-Region Characteristics**



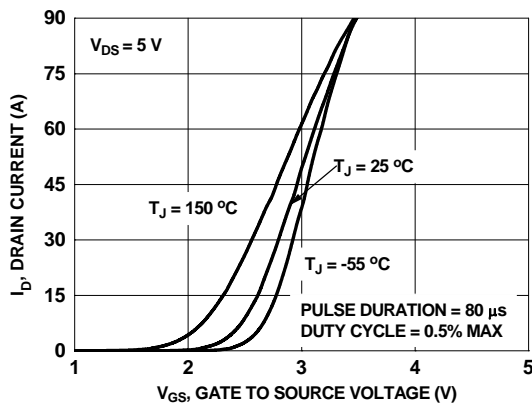
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



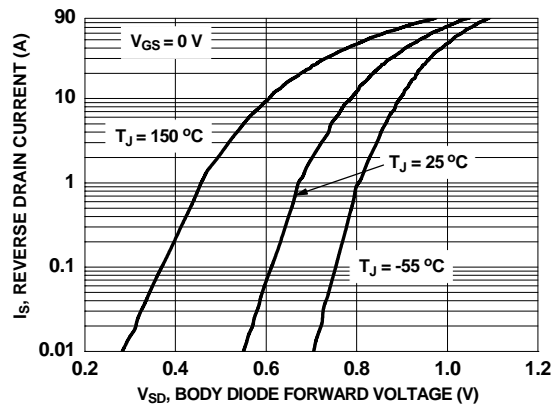
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

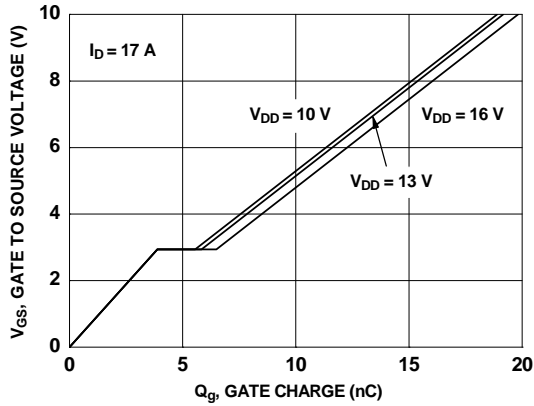


**Figure 5. Transfer Characteristics**

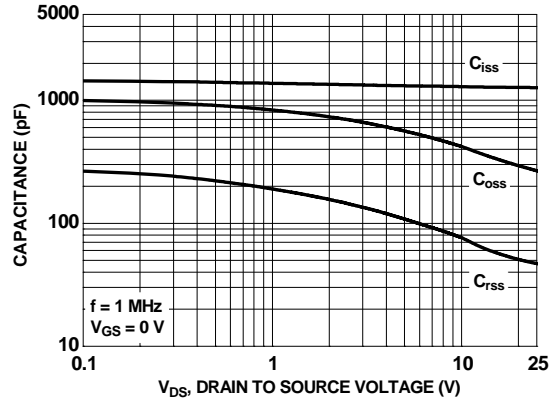


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

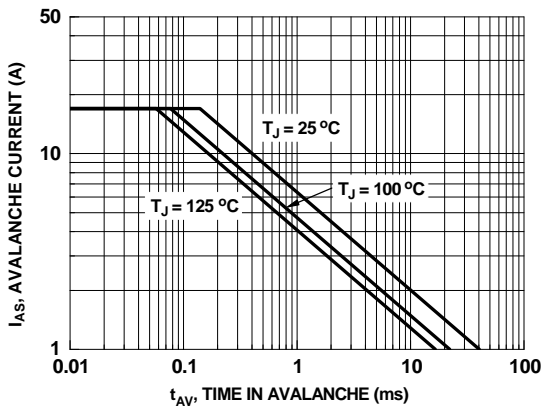
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



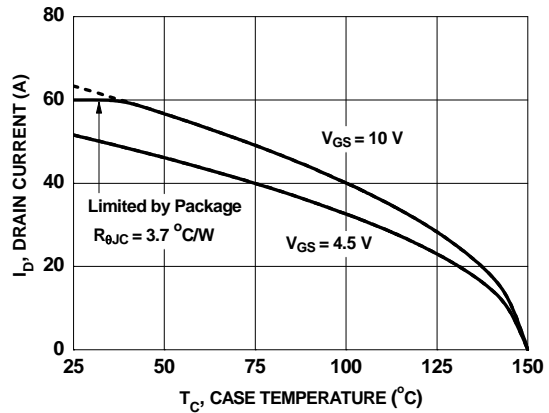
**Figure 7. Gate Charge Characteristics**



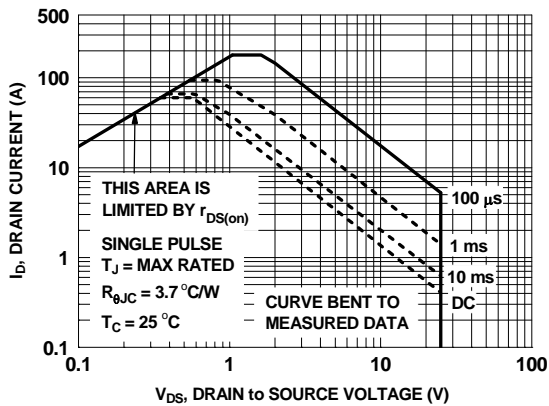
**Figure 8. Capacitance vs Drain to Source Voltage**



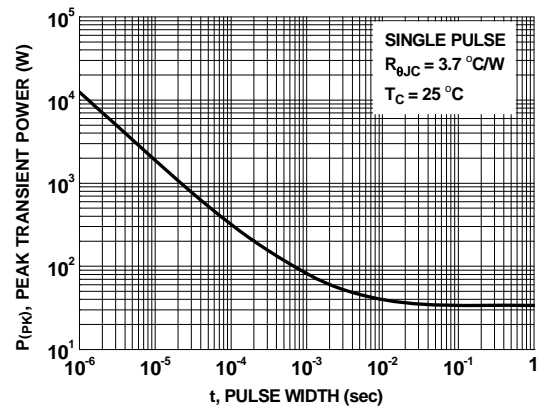
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

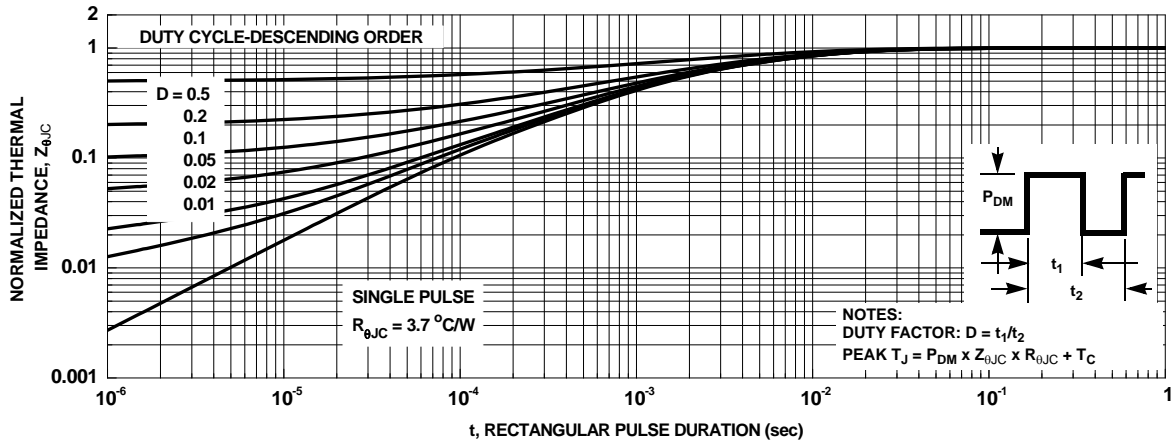


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

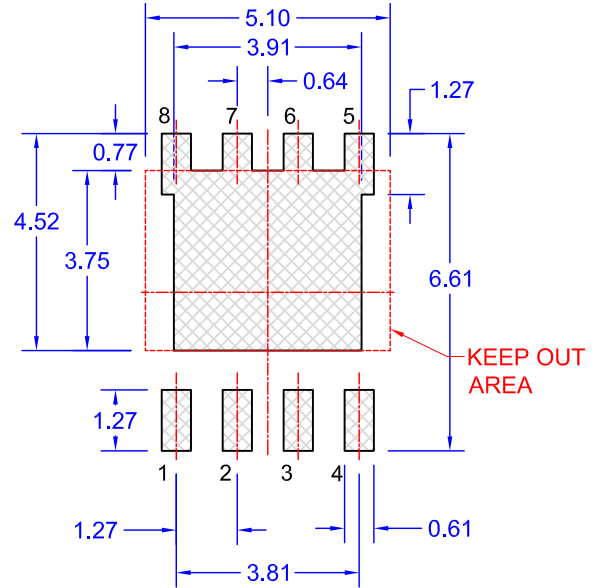
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**



TOP VIEW



LAND PATTERN RECOMMENDATION

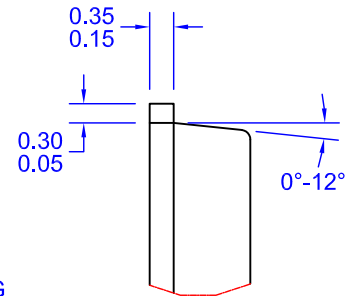


SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV10



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